ADS 2016
SIPro / PIPro
Technology Overview

KEYSIGHT TECHNOLOGIES

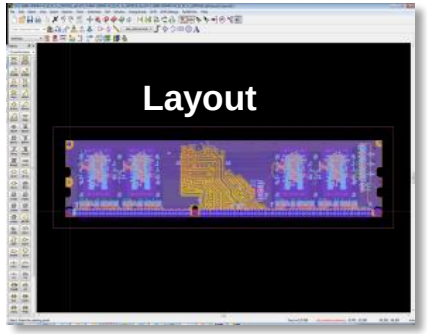
ADS: SIPro and PIPro

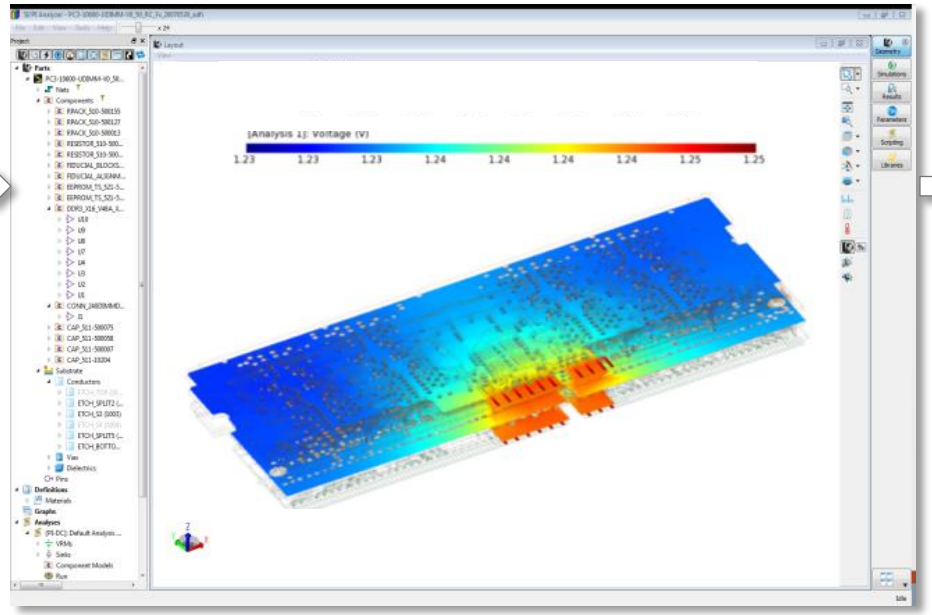
A Cohesive Workflow for SI and PI Analyses

Layout Import into ADS
(Direct *.brd Import, Allegro ADFI or ODB++ flow)

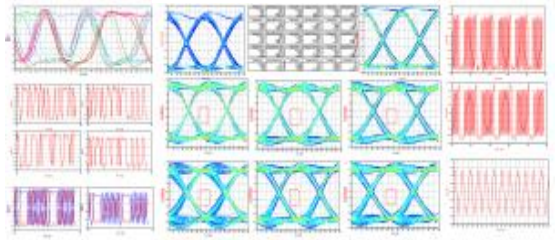
SIPro / PIPro Analysis

Transient Convolution
Channel Sim
DDR Bus Sim





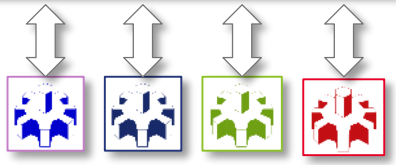
ADS Schematic



Set up and run analyses

Manage nets, VRMs, sinks, components

3D layout view and results visualization



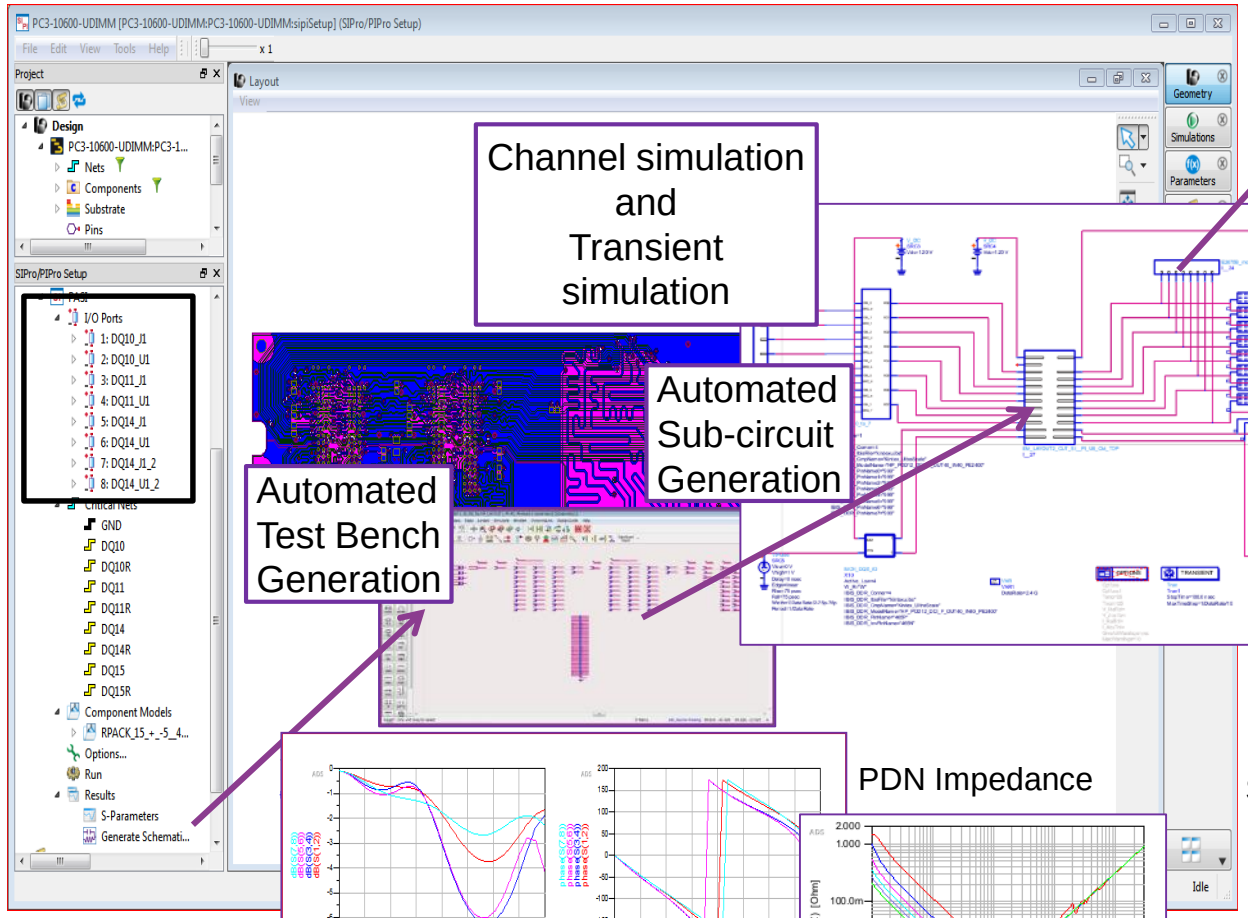
4 New EM Simulators

PI-DC	PI-AC	Power Plane	Power-Aware Signal
IR Drop	PDN Impedance	Resonances	Integrity

KEYSIGHT TECHNOLOGIES

Increased Productivity for Post-layout Analysis

Seamless flow from EM-analyses back into schematic for both SI and PI



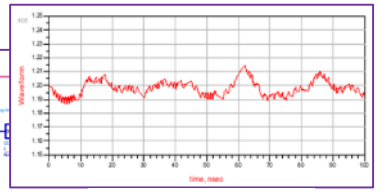
I/O ports

Channel simulation and Transient simulation

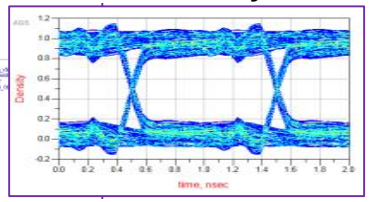
Automated Sub-circuit Generation

Automated Test Bench Generation

Decap Tuning, Optimization, Circuit-level VRM modeling



SSN Analysis



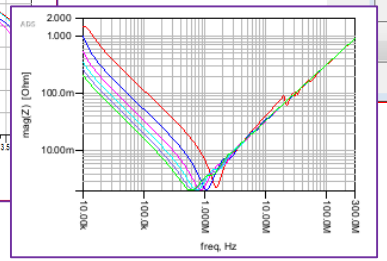
Data with VCC Bounce

DDR4 Low BER Simulation

And More Simulation!

Compliance Test

PDN Impedance

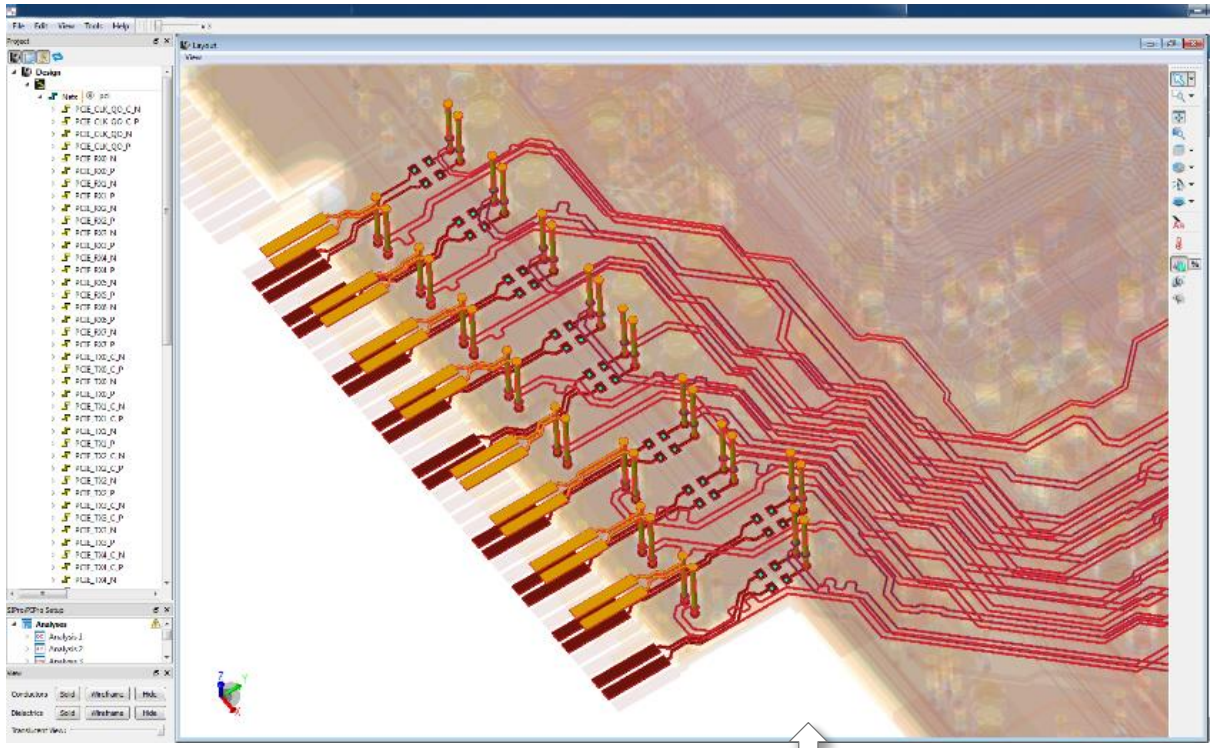


S-parameter Extraction

SIPro

Simulation Technology Overview

A composite technology of fast FEM + Planar EM



Power-Aware
Signal Integrity

- **Speed *and* Accuracy**

A purely EM-based simulation, capturing more EM effects than 2D-hybrid solutions

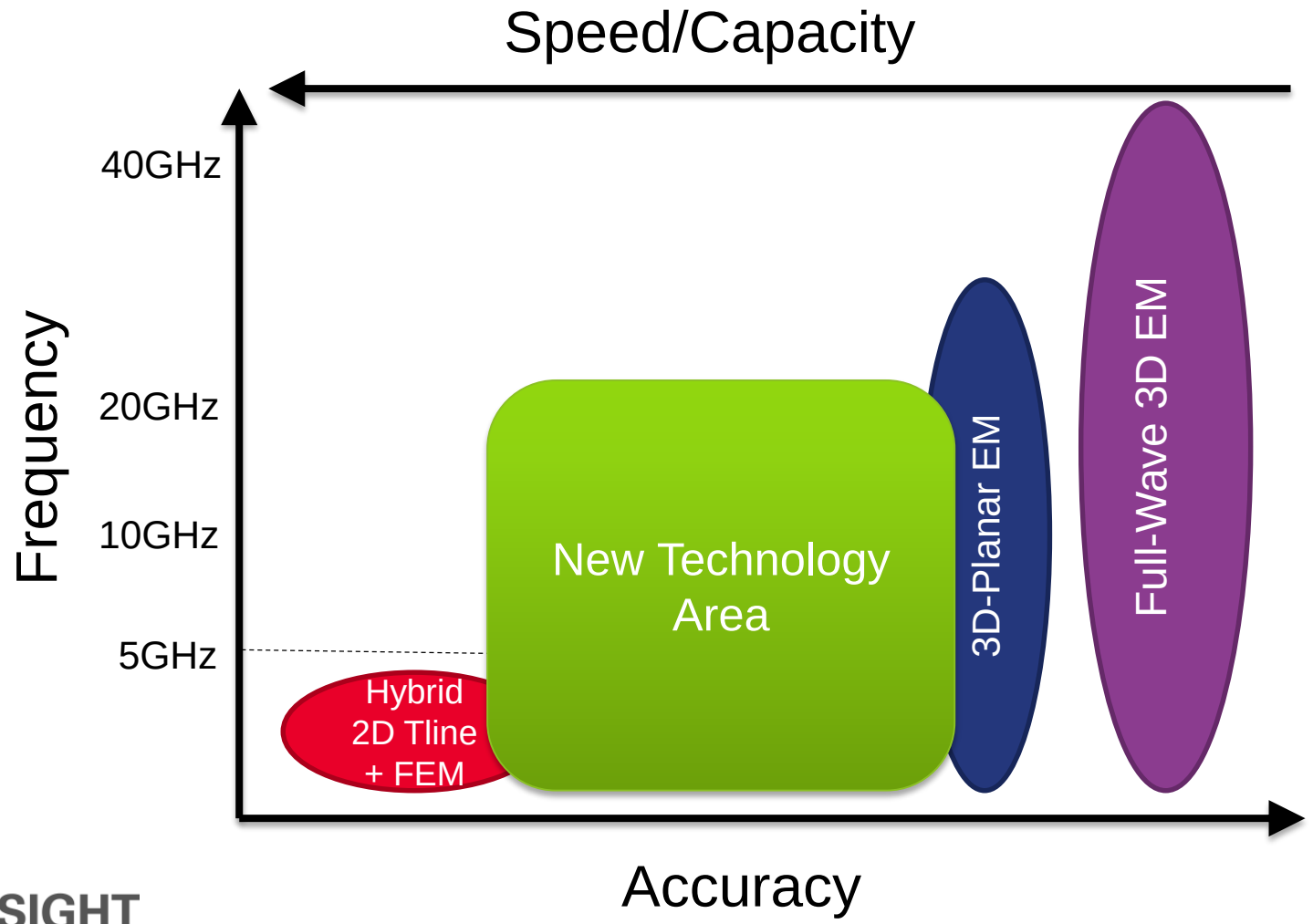
- **SI-specific, net-driven use-model and flow**
- **Easily plot Transmission, Return loss, Xtalk and TDR/TDT**
- **Automatic-schematic generation**

EM model flows back to schematic ready for further simulation with Transient, Channel Sim, DDR Bus Sim and more

KEYSIGHT TECHNOLOGIES

SIPro

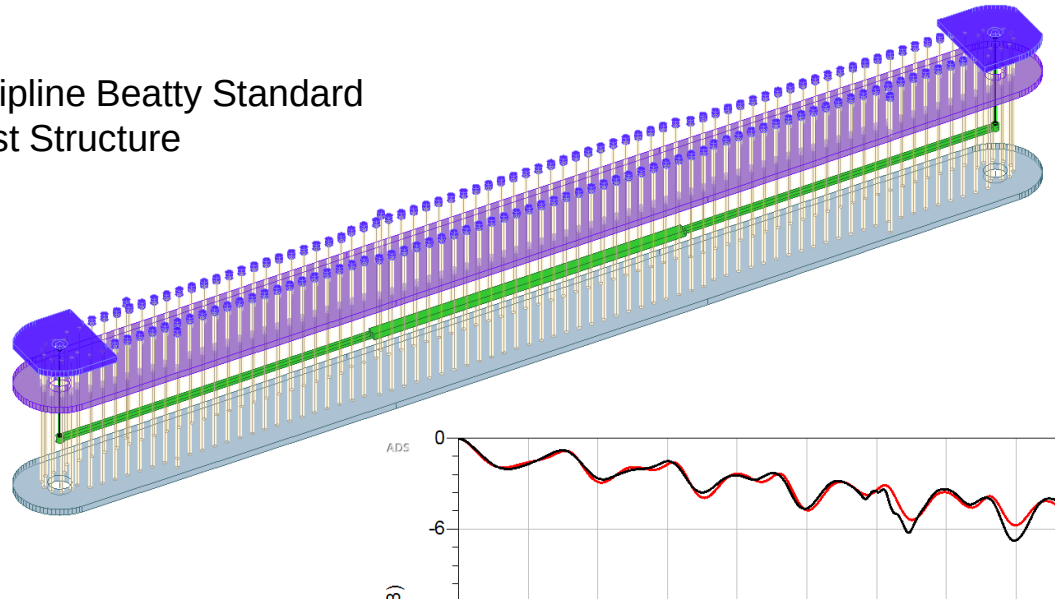
Simulation technology comparison for high-speed digital PCBs

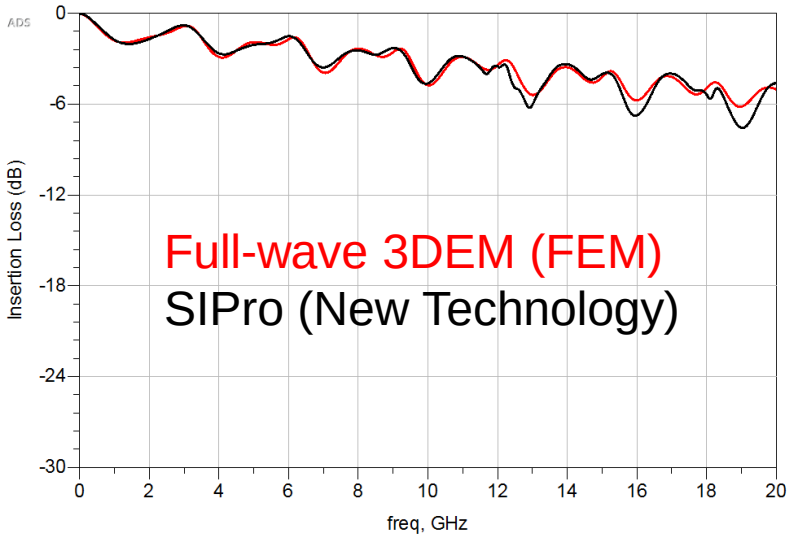


SIPro: Accuracy

Simulation comparison from Wild River Technology test case

Stripline Beatty Standard
Test Structure

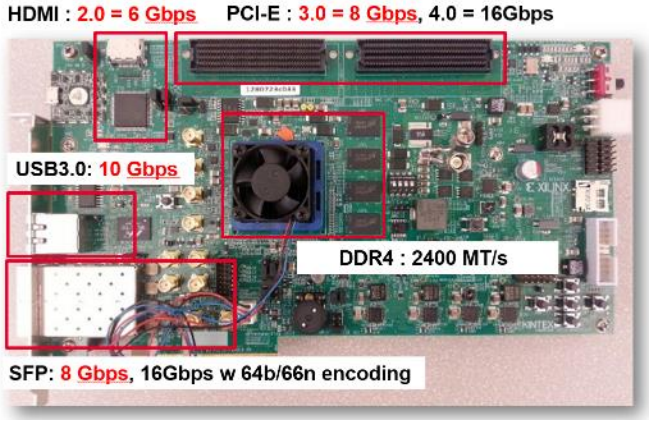




Wild River Technology
CMP-28 SI Kit

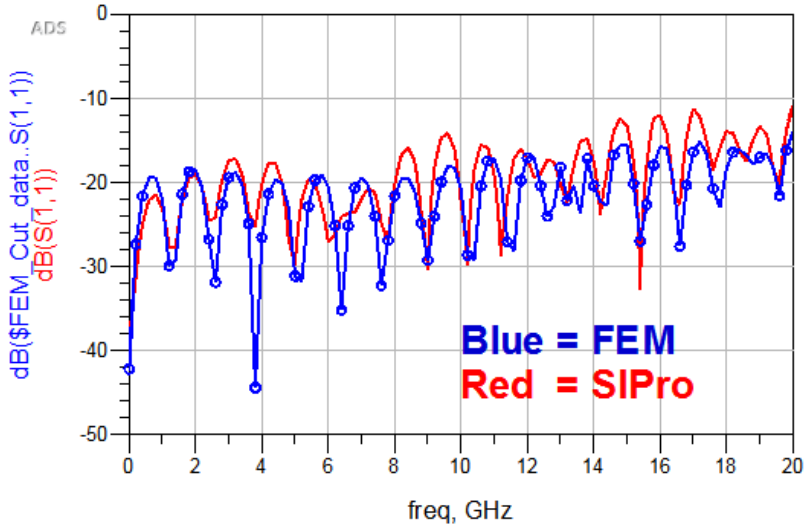
SIPro: Speed *and* Accuracy

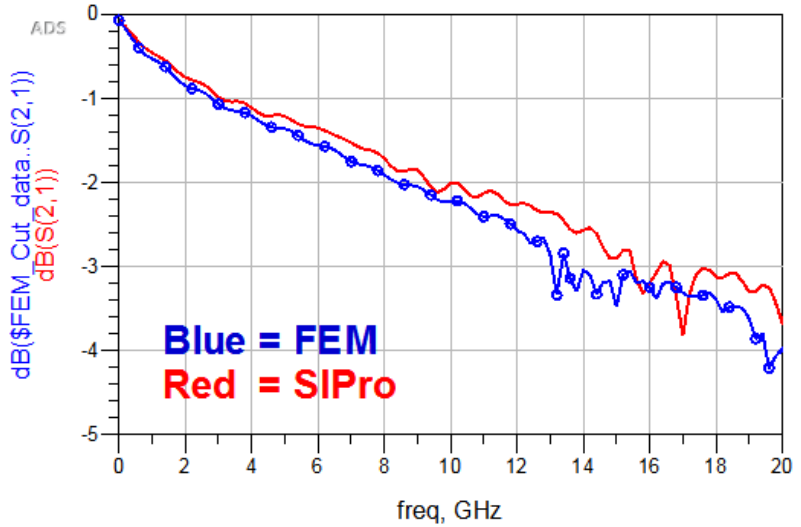
Xilinx KCU105 FPGA Platform Board



– Example : SFP (Small Form Factor Pluggable) TX channel

S11 Very good agreement! **S21**





– SIPro finished in 18 min, a fraction of simulation time compared to FEM

- **SIPro:** **1GB memory, 6 secs per frequency point**
- **FEM:** **8GB memory, 12 mins per point**

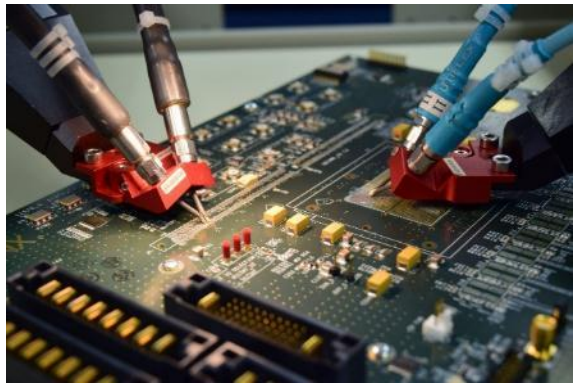
KEYSIGHT TECHNOLOGIES

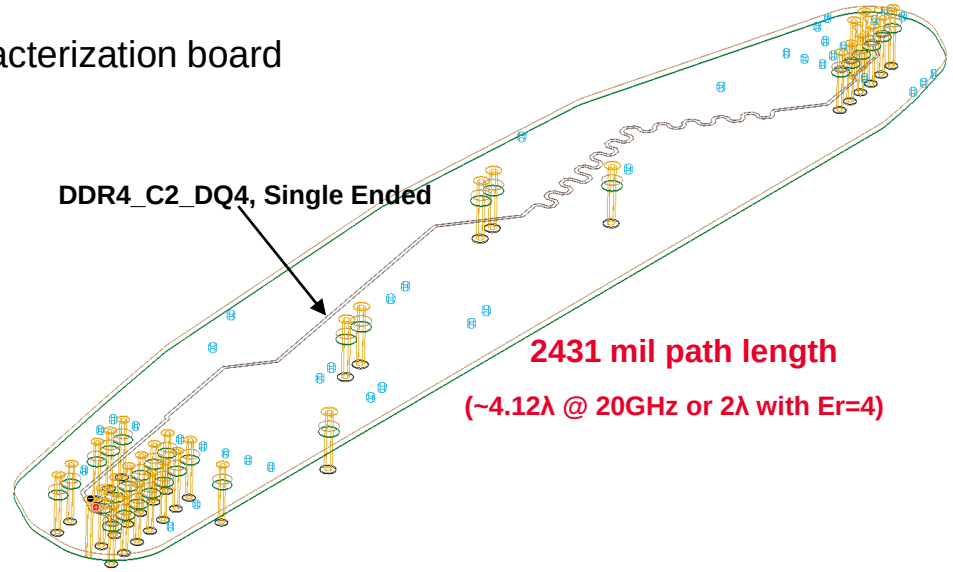
SIPro: Accuracy

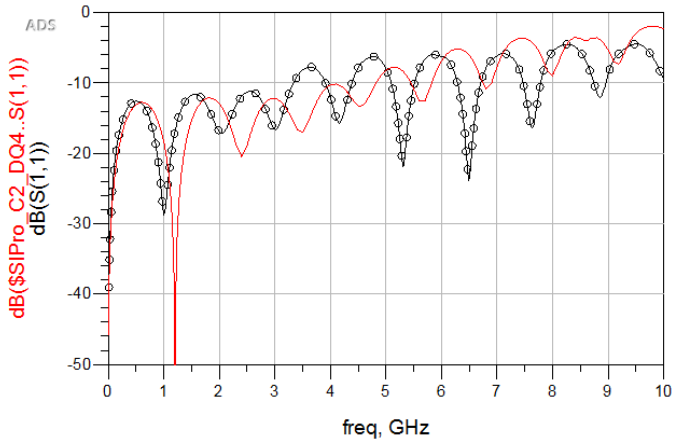
DDR4 DQ Channel, Measured vs SIPro

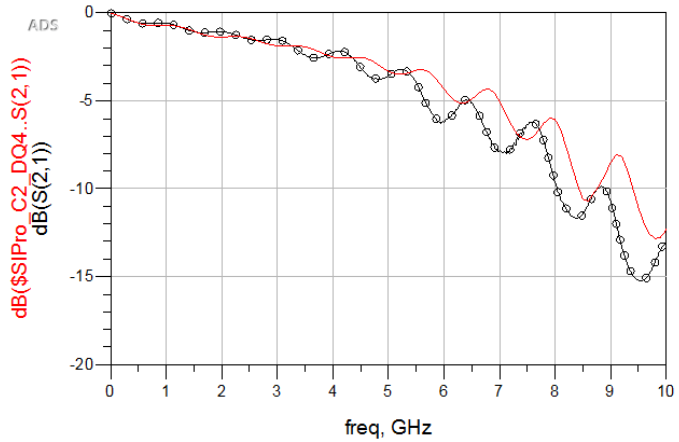
- 28-layer Xilinx UC1650B DDR4 memory characterization board
- DDR4_C2_DQ4 single ended line (cookie cut)

Measurement: Courtesy of GigaTest Labs









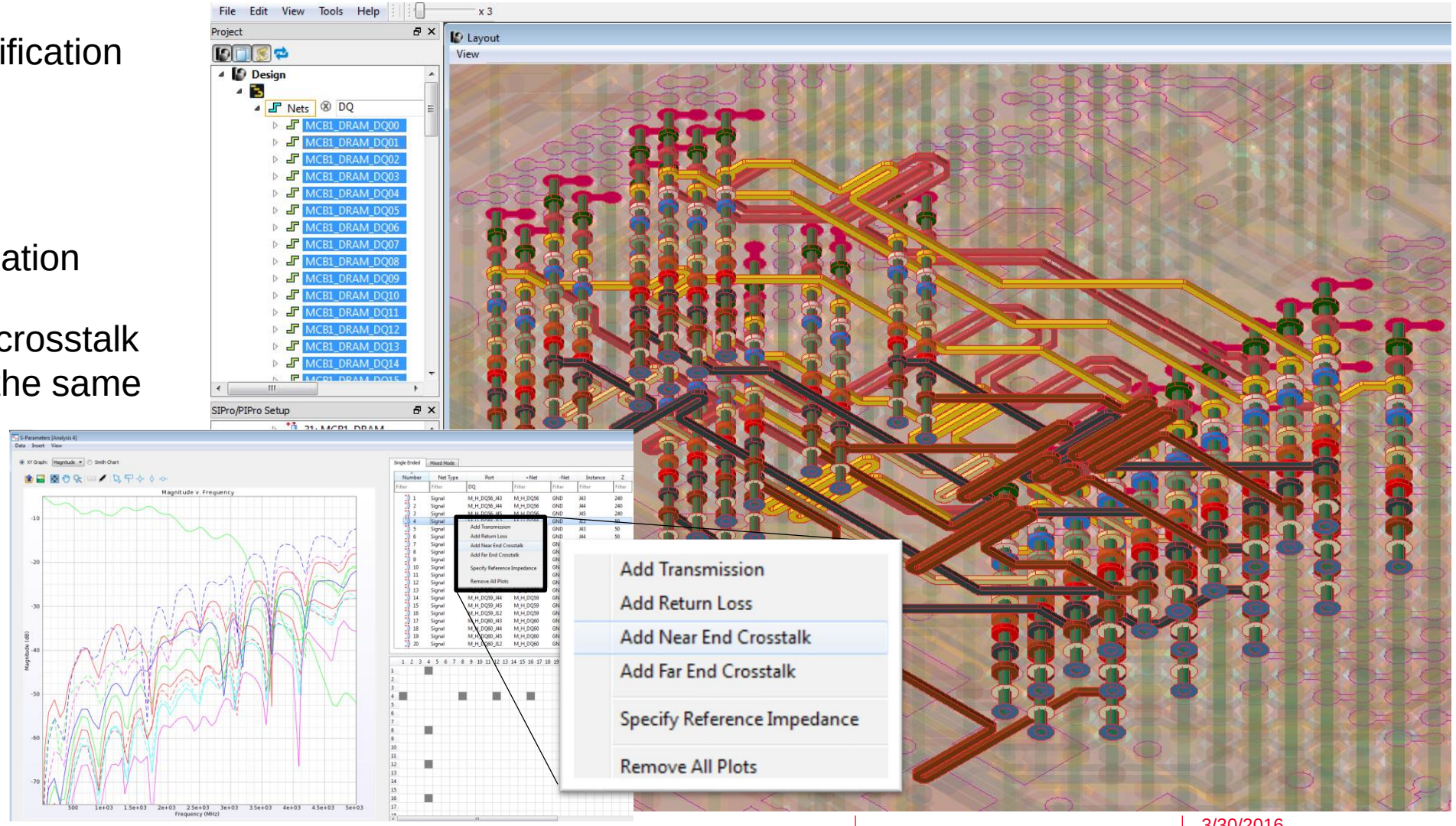
Er as specified by the designer,
not 'as fabricated'

Red = SIPro **Black = Measured**

SIPro: SI-specific use-model and flow

Layout to results in less than 20 clicks…

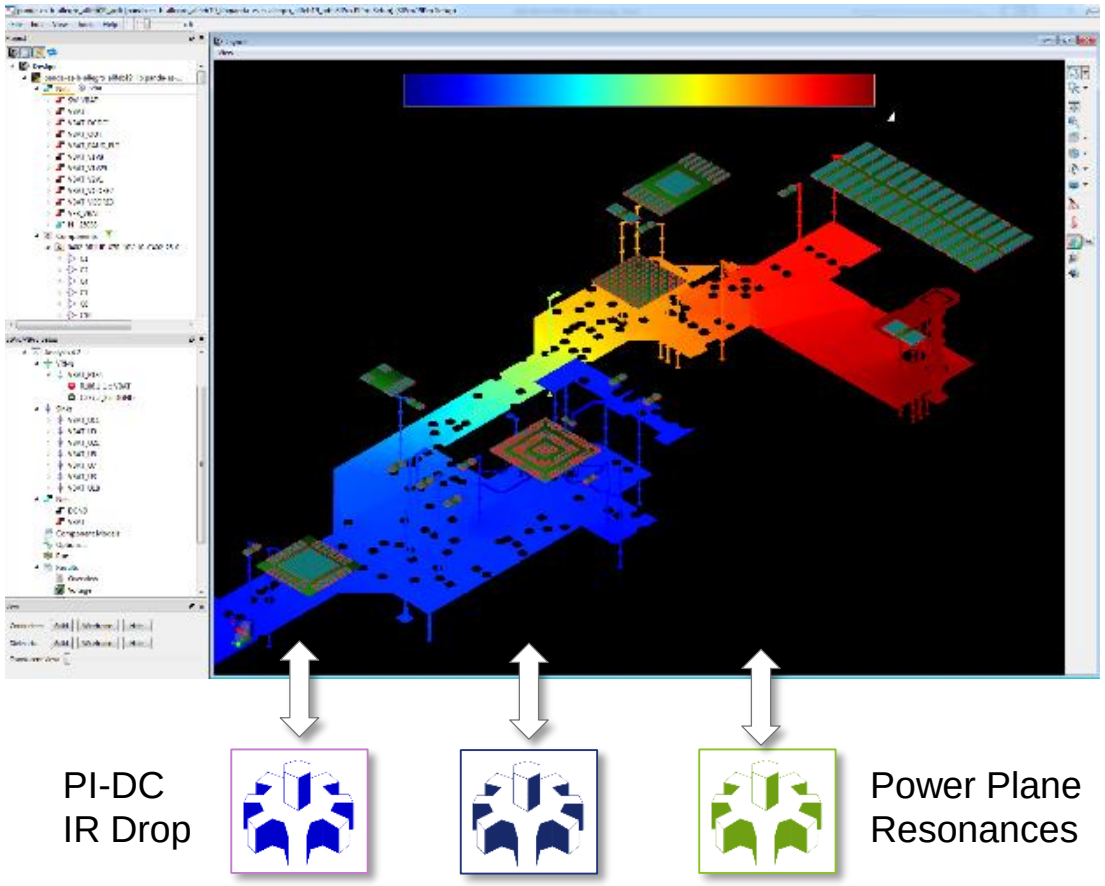
- No layout simplification required!
- Net-driven
- Guided port creation
- Quickly plot all crosstalk elements from the same component
- Easily plot TDR/TDT
- Mixed-mode S-parameters



PIPro

Simulation Technology Overview

PIPro has an efficient net-driven PI analysis setup with 3 new simulator engines



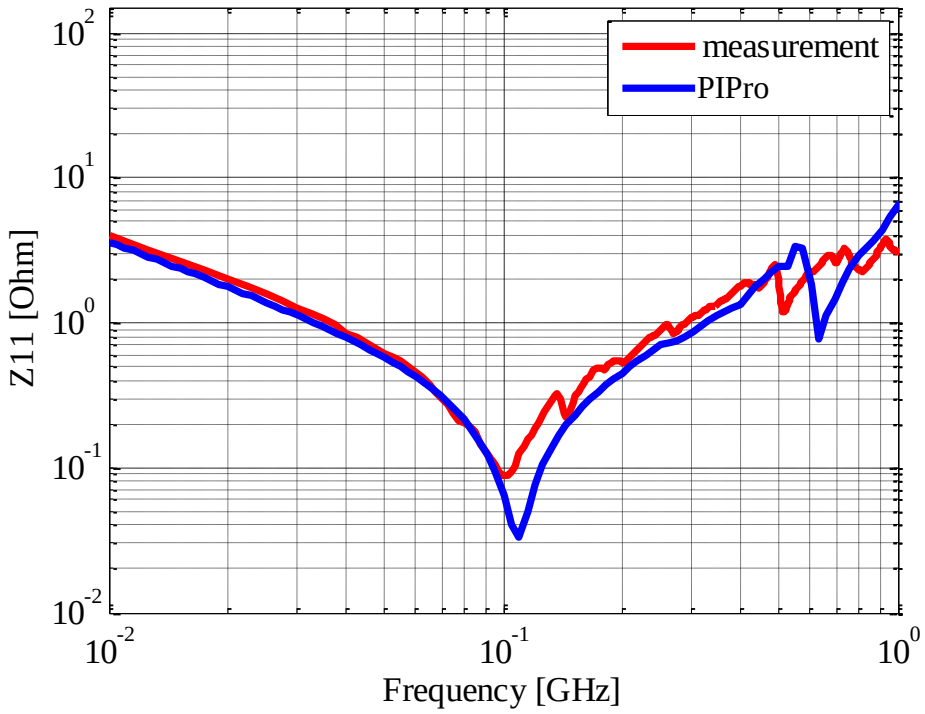
- **Speed *and* Accuracy**
- **PI-specific net-driven use-model and flow**
- **Change decap values/models without needing to re-simulate**
- **Automatic-schematic generation**

EM model flows back to schematic ready for further simulation with behavioral and circuit-level simulations of VRMs, sinks and more

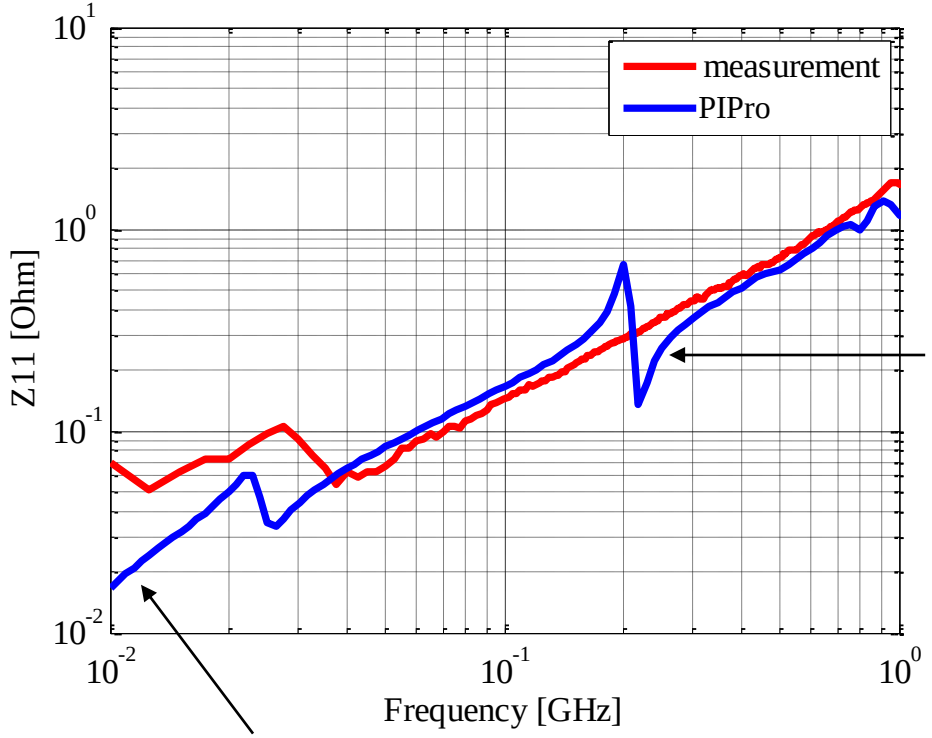
PIPro: Accuracy

Customer validated test-case, Simulation vs. Measured Data

Bare-Board



PDN populated with Decaps



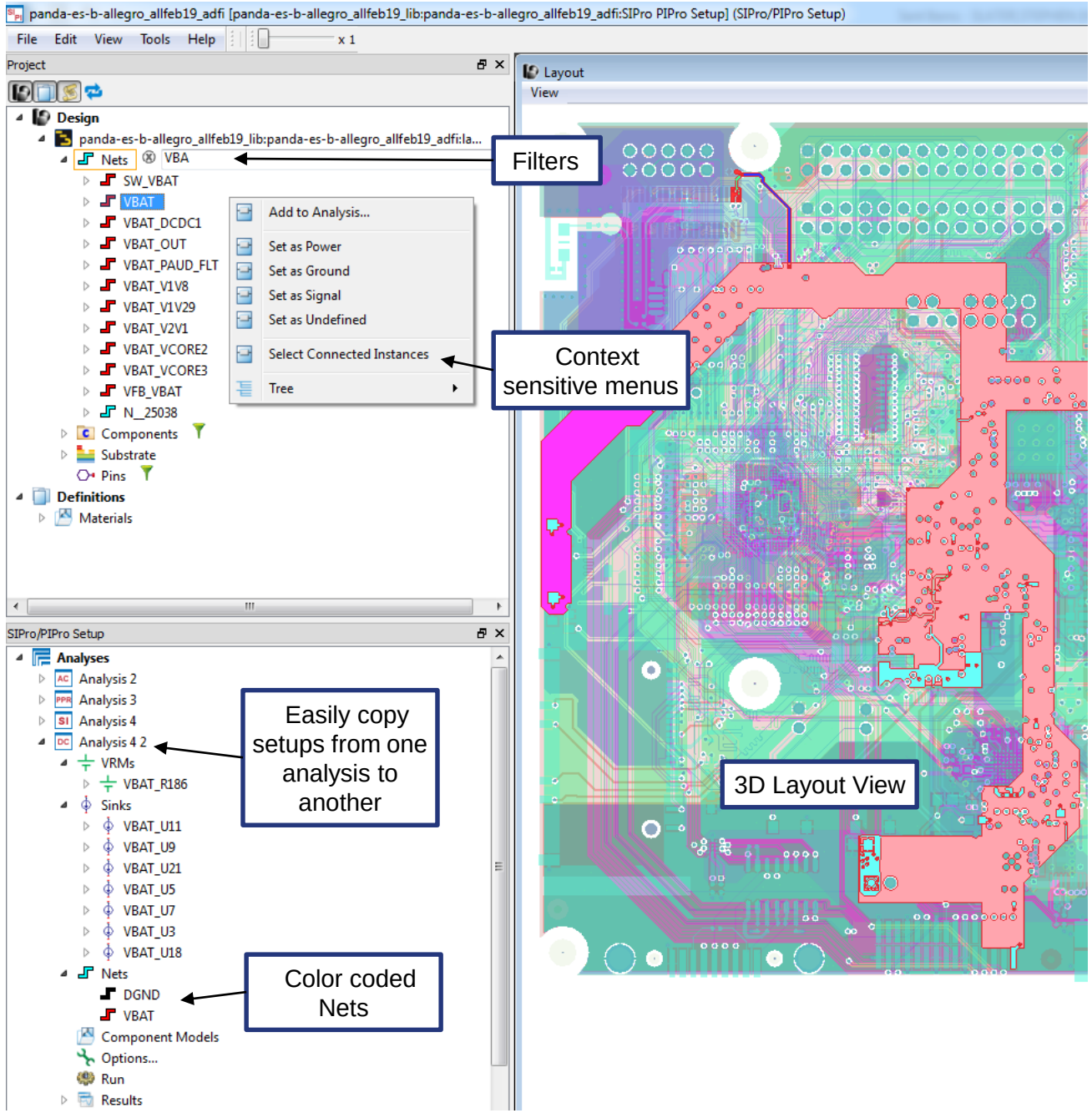
Customer used ideal cap values with no ESR specified, hence sharp resonances.

Ideal VRM model.
Customer did not have IC data.

Test case:
ATE test card – PDN traverses many layers

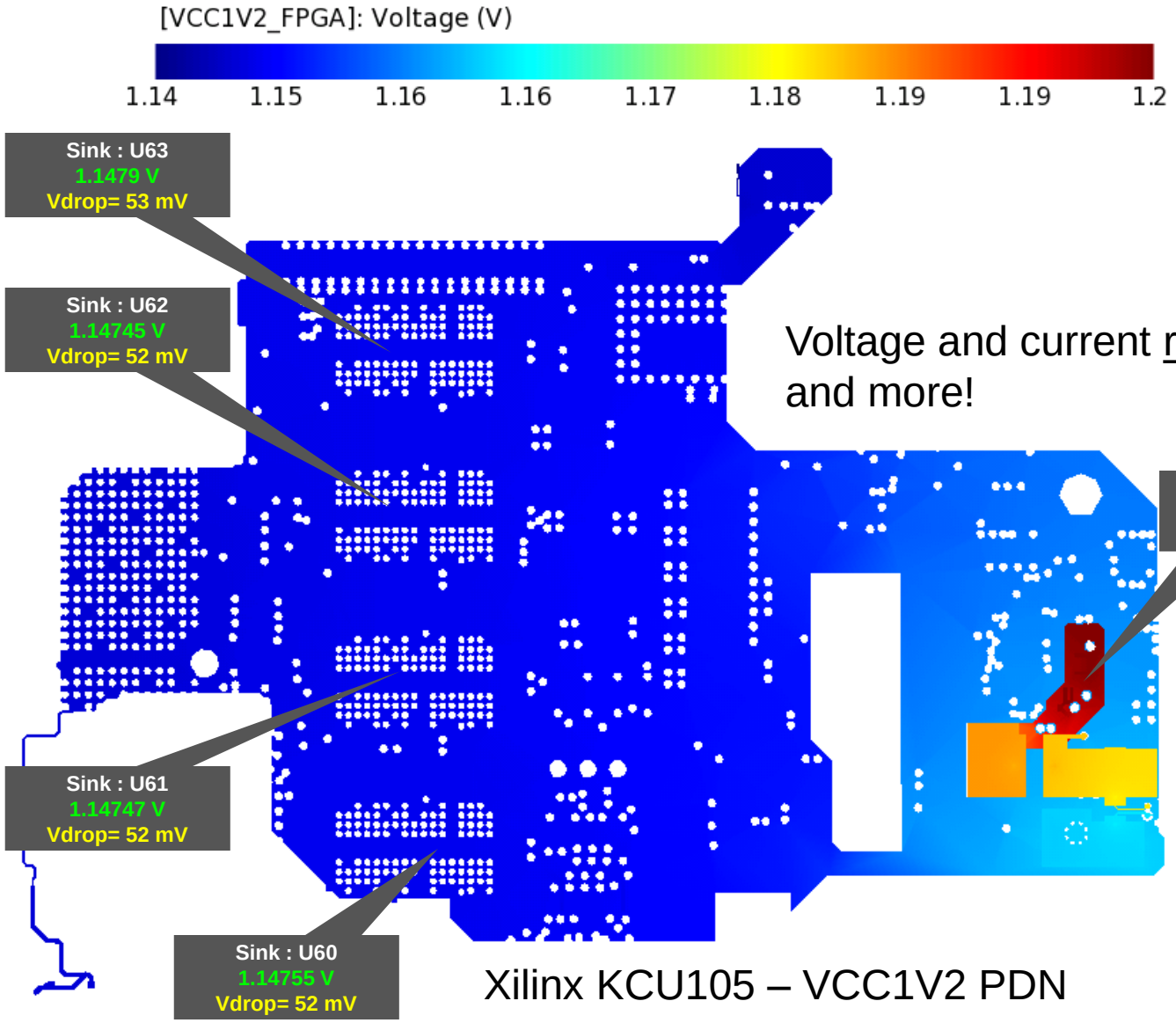
Designed for Usability

- Filter by Net
- Filter by Component
- Right-click to add-to-analysis
- Drag & Drop
- Hierarchical search for complex selections
- Context sensitive menus e.g. *'Select instances connected to ONLY the selected nets'*



KEYSIGHT TECHNOLOGIES

PIPro – DC IR Drop



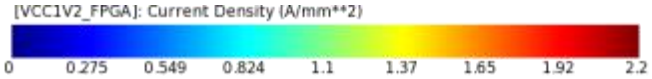
SINKs

Name	Source Current	VRM Voltage	Input Voltage	Tolerance	Margin	Pass/Fail
VCC1V2_FPGA_U60	0.3 A	1.2 V	1.14755 V	5 %	0.00755 V	pass
VCC1V2_FPGA_U61	0.3 A	1.2 V	1.14749 V	5 %	0.00749 V	pass
VCC1V2_FPGA_U62	0.3 A	1.2 V	1.14745 V	5 %	0.00745 V	pass
VCC1V2_FPGA_U63	0.3 A	1.2 V	1.14747 V	5 %	0.00747 V	pass
VCC1V2_FPGA_U1	0.8 A	1.2 V	1.1463 V	5 %	0.0063 V	pass
VCC1V2_FPGA_U24	0.4 A	1.2 V	1.14094 V	5 %	0.00094 V	pass
VCC1V2_FPGA_U41	0.3 A	1.2 V	1.14687 V	5 %	0.00687 V	pass
VCC1V2_FPGA_U42	0.3 A	1.2 V	1.14715 V	5 %	0.00715 V	pass

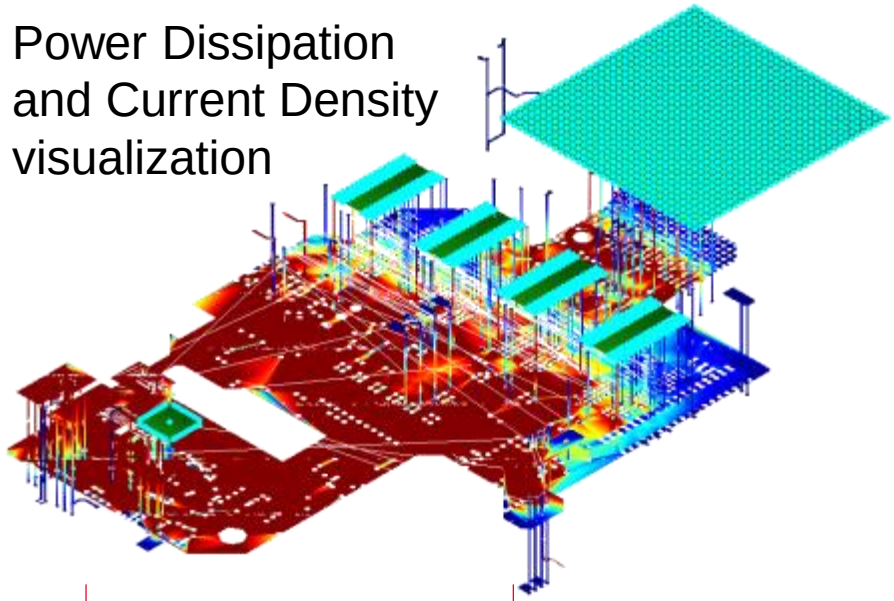
VRMs

Name	Source Voltage	Output Voltage	Output Current	Tolerance	Margin	Pass/Fail
VCC1V2_FET_SWITCH_U4	1.2 V	1.2 V	-2.99999 A	5 %	0.06 V	pass

Voltage and current reported per Via, Sink, VRM and more!



Power Dissipation and Current Density visualization



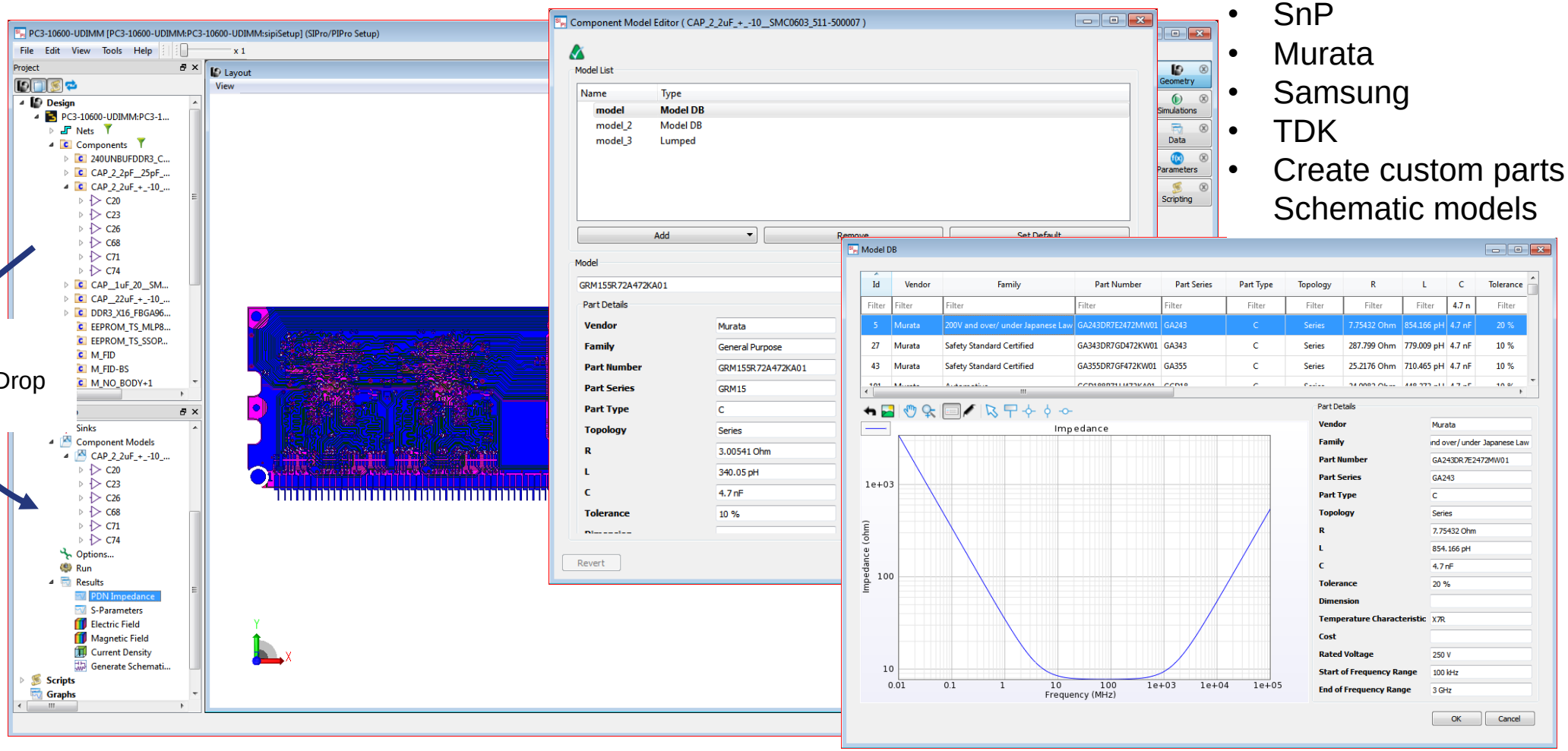
Xilinx KCU105 – VCC1V2 PDN

PIPro – AC PDN Impedance Analysis

Component Model assignment:

- Lumped
- SnP
- Murata
- Samsung
- TDK
- Create custom parts from Schematic models

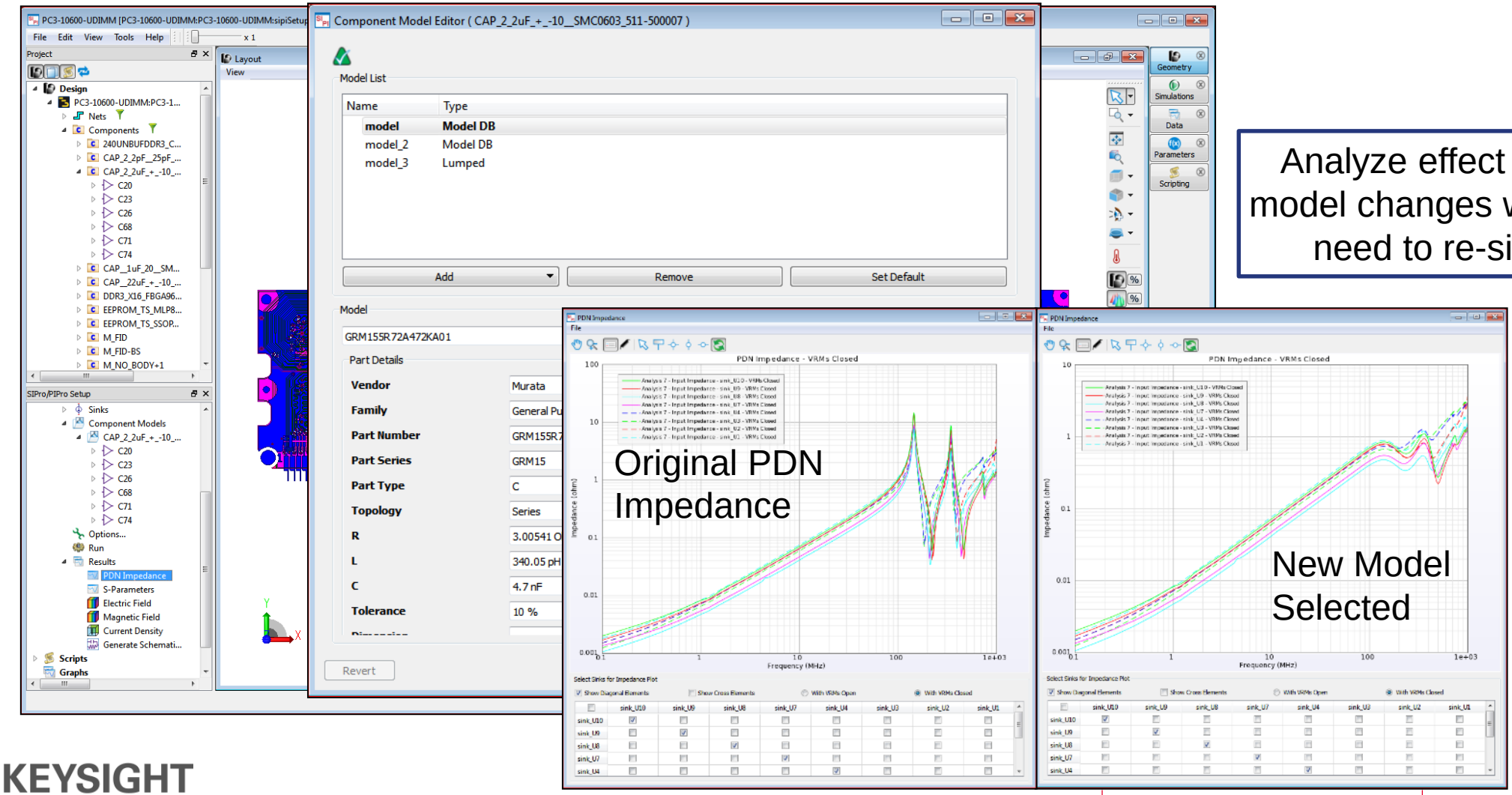
Easy setup:
Filter, drag and Drop Components



+ Full scripting support for setup, simulation and post-processing

PIPro – AC PDN Impedance Analysis

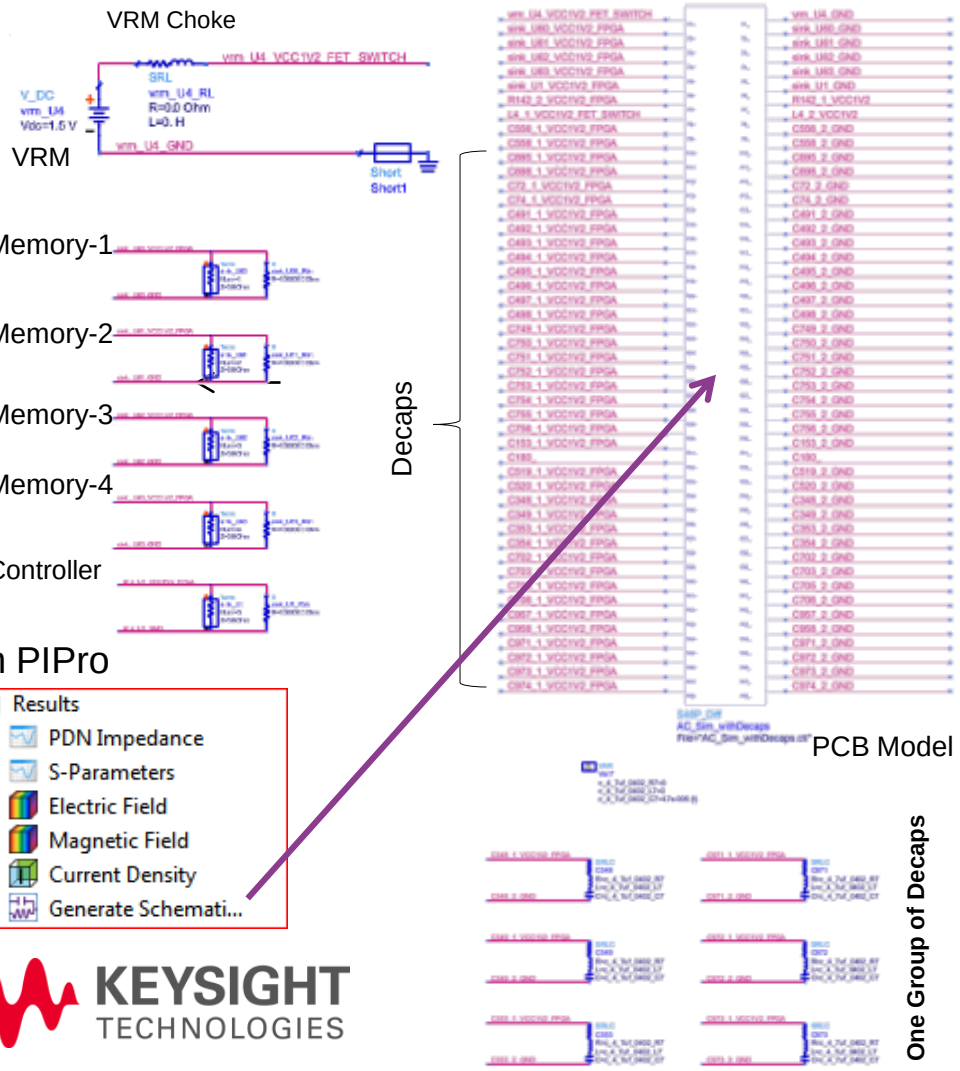
Decap Selection in PIPro



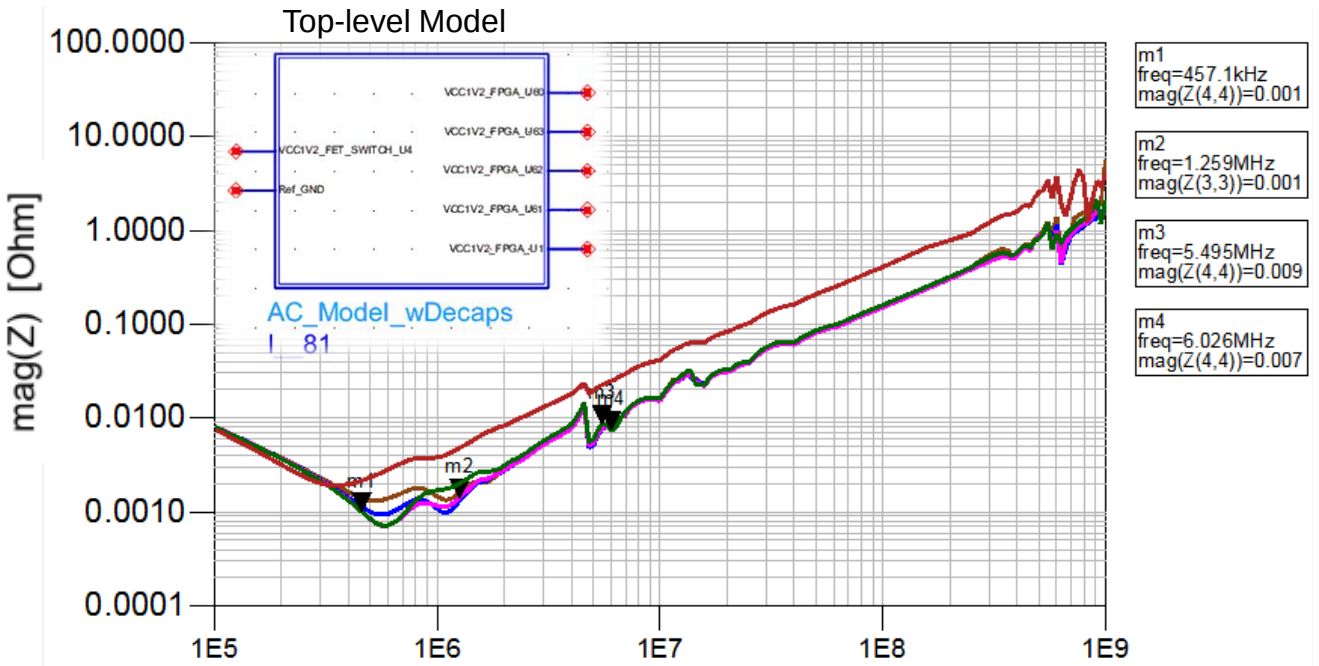
Analyze effect of decap model changes without any need to re-simulate

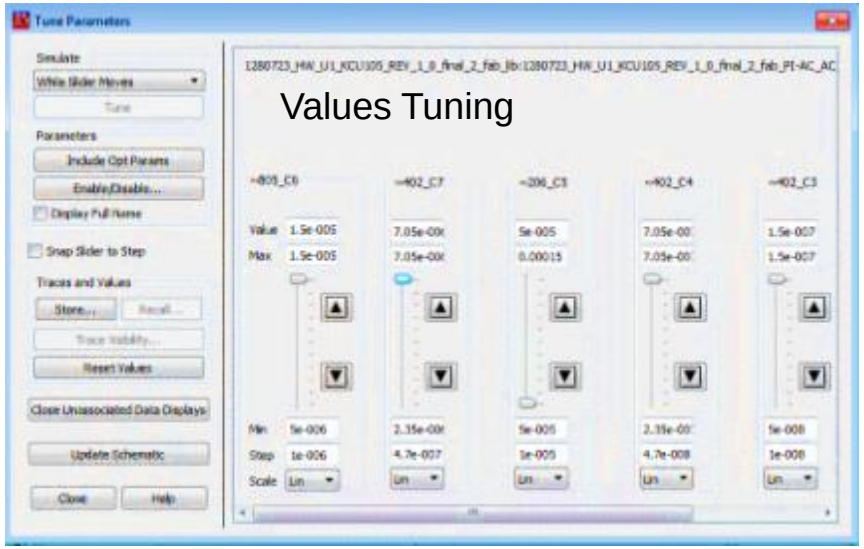
PIPro – AC PDN Impedance Analysis

Decap tuning from schematic



From PIPro



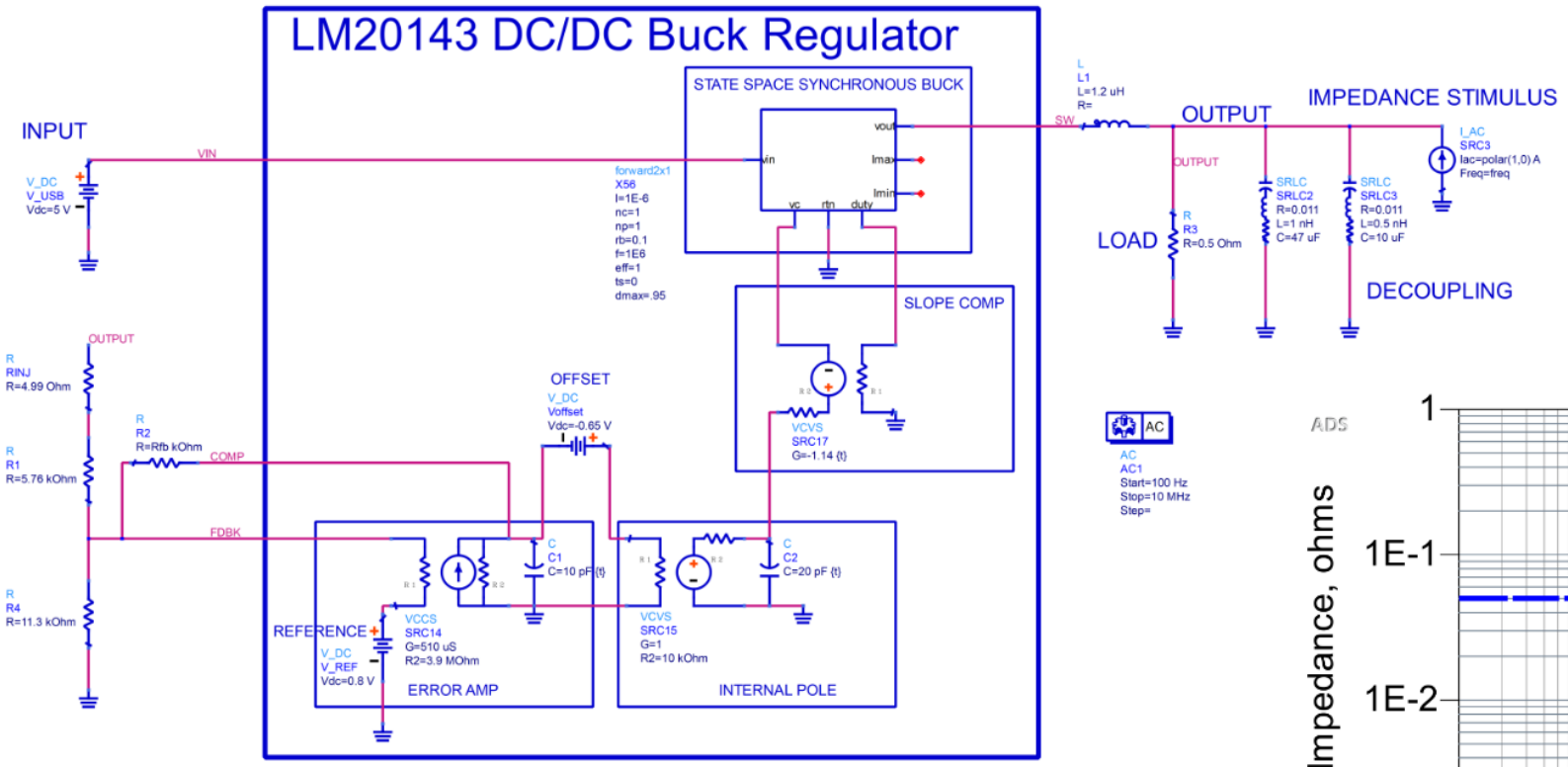


Completely flexible PDN optimization strategy

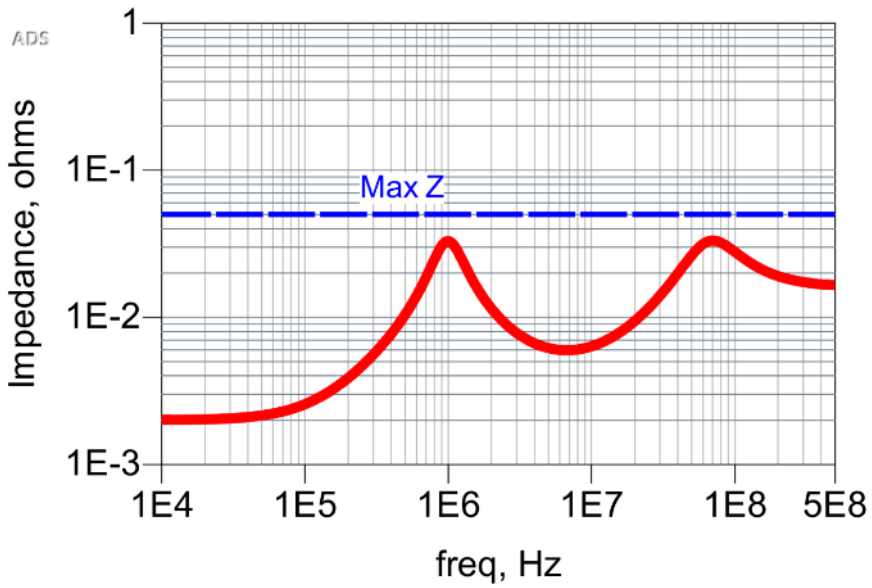
KEYSIGHT TECHNOLOGIES

PIPro – The power of the workflow

Including the DC-DC converter in the Simulation



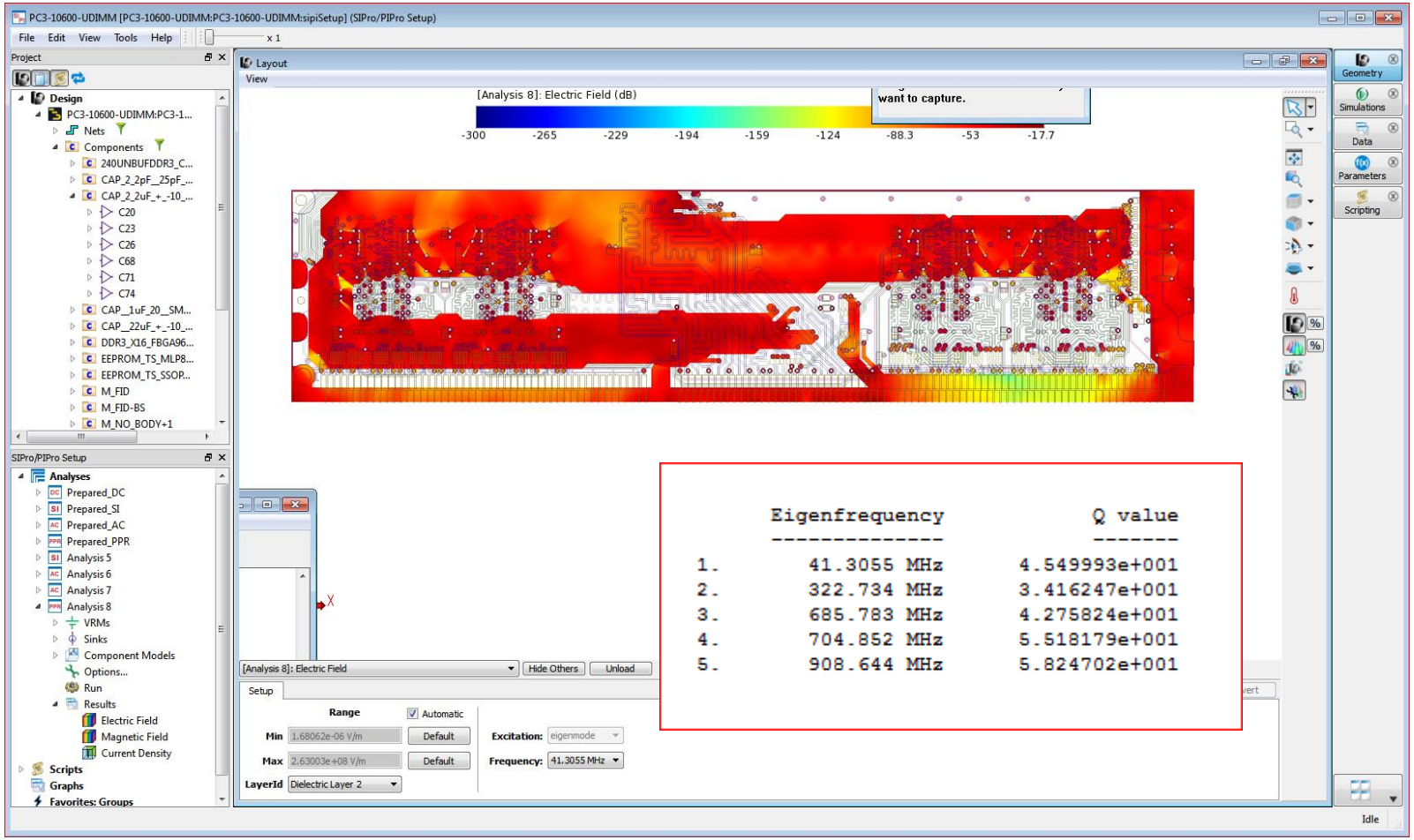
- Behavioral representations of VRM together with EM-model of the PDN, to analyze true performance with feedback
- Circuit-level modeling for Power Supply design



KEYSIGHT TECHNOLOGIES

PIPro – Power Plane Resonance Analysis

Self resonances



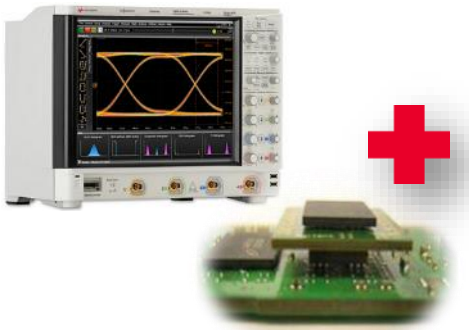
	Eigenfrequency	Q value
1.	41.3055 MHz	4.549993e+001
2.	322.734 MHz	3.416247e+001
3.	685.783 MHz	4.275824e+001
4.	704.852 MHz	5.518179e+001
5.	908.644 MHz	5.824702e+001

Analyze self-resonances of the PCB and inspect trouble areas that have the highest field strength

Summary

ADS 2016: SIPro / PIPro New Features

- SIPro: Innovative new composite EM technology
- Speed *and* Accuracy
- A cohesive workflow for SI and PI analyses



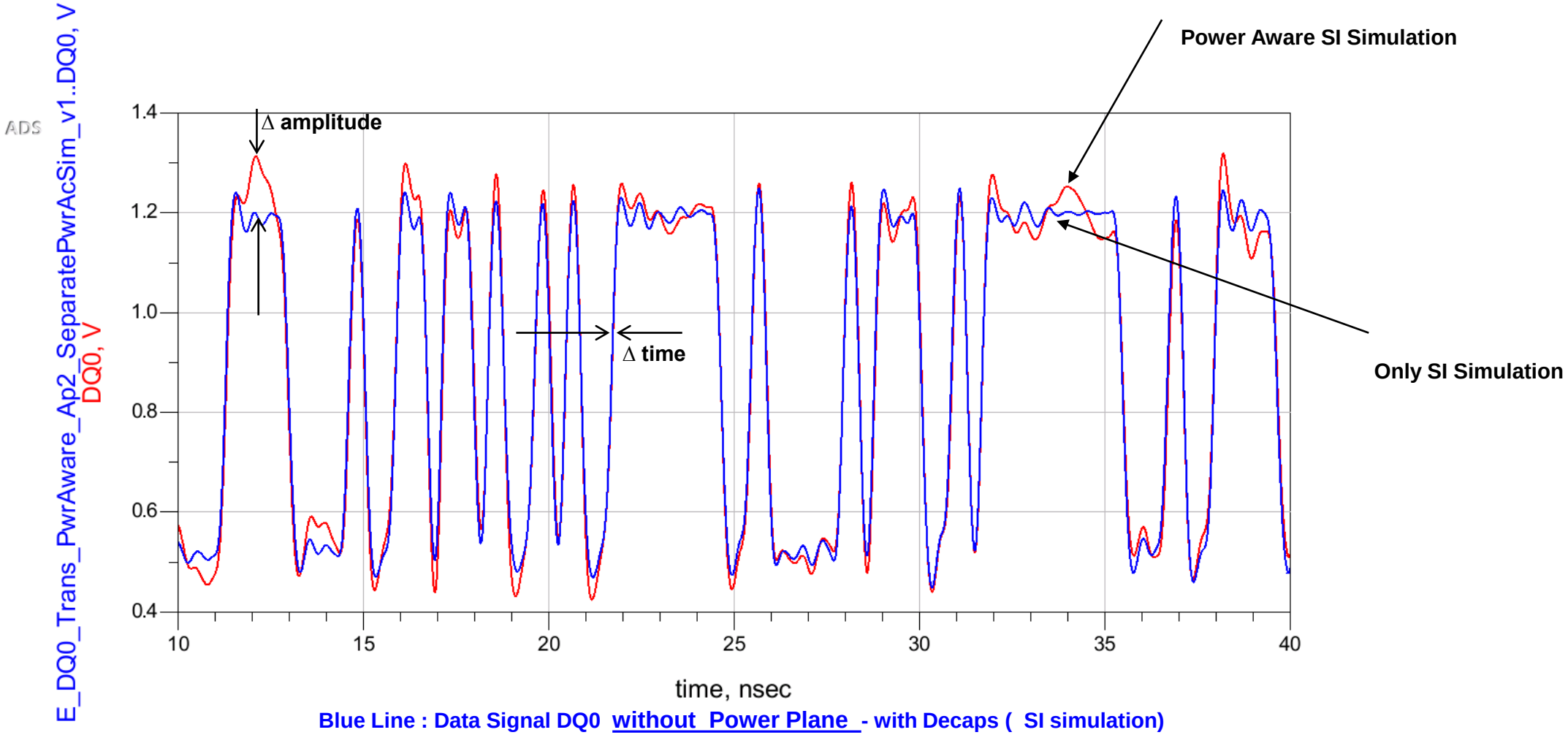
Hardware

Software

People

Appendix

Power Aware SI Simulation : Data Signal (DQ0) with and without Power Plane (with Decaps)



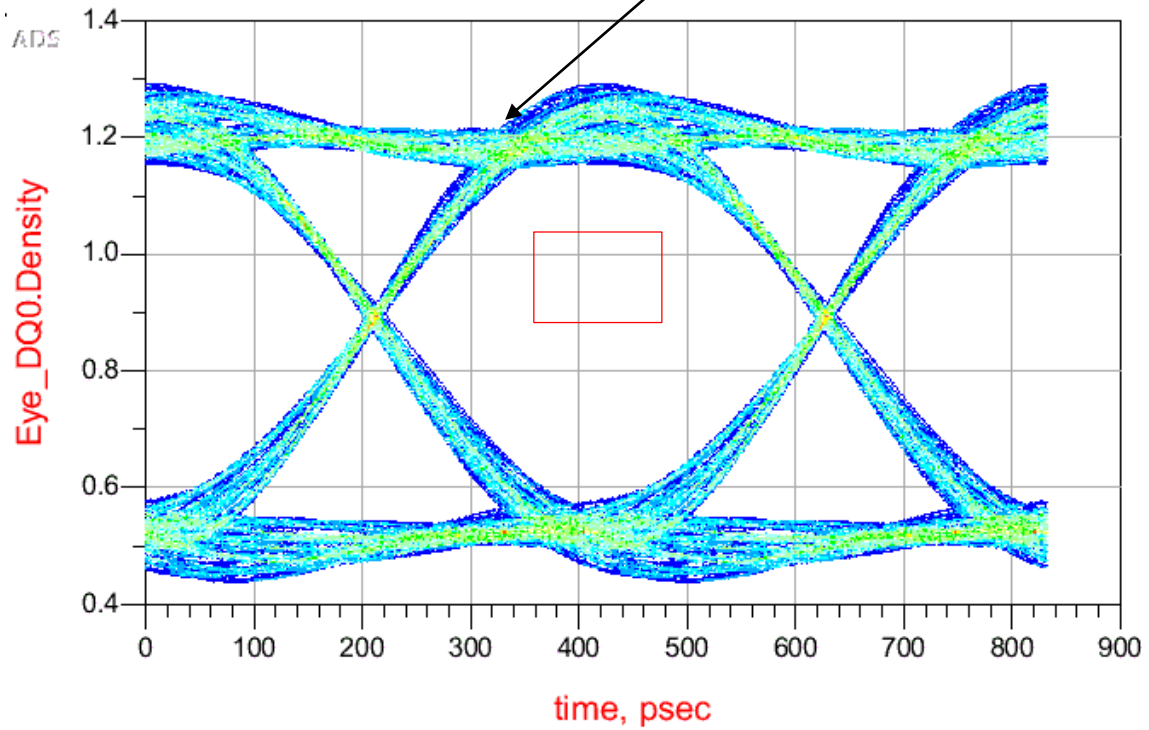
Blue Line : Data Signal DQ0 without Power Plane - with Decaps (SI simulation)

Red Line : Data Signal DQ0 in presence of Power Plane – with Decaps (Power Aware SI Simulation)

KEYSIGHT TECHNOLOGIES

Power Aware SI Simulation : Data Signal (DQ0) with and without Power Plane (with Decaps)

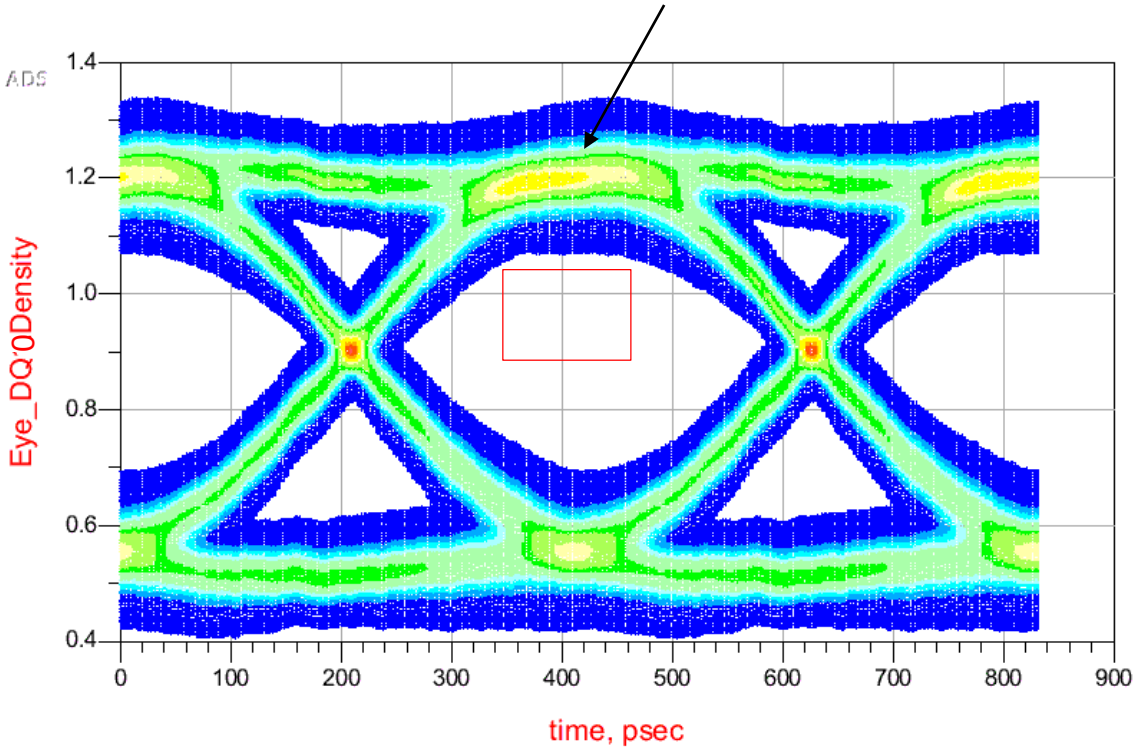
Only SI Simulation (no Power nets effect) in simulation



Eye Diagram without taking effect of Power Net

Eye is more open

<u>Power Aware SI Simulation</u> taking Power nets in simulation

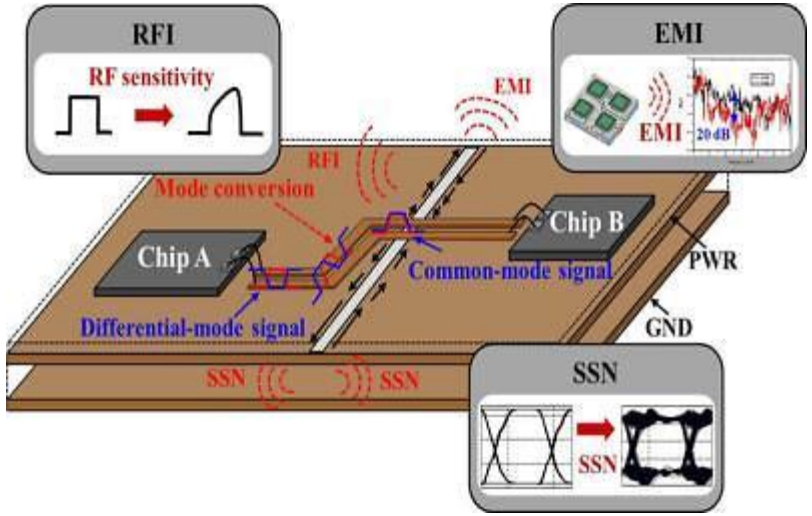


Eye Diagram with Power Net **<u>(Power Aware SI</u>**)

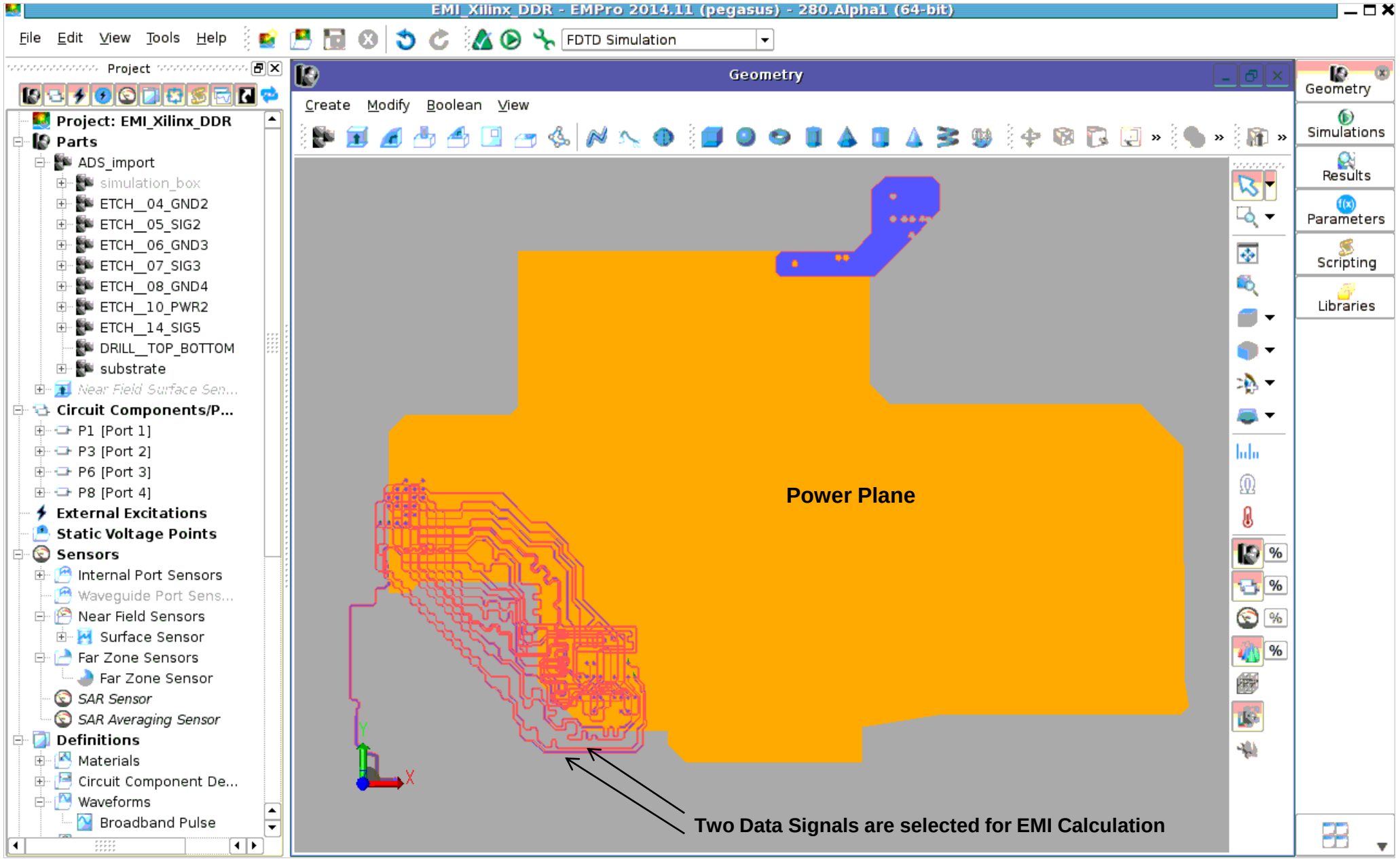
EMI/ EMC Analysis

Objective

1. EMI Analysis of DDR4 Data Signal
2. EMI Analysis in EMPro using Power Aware waveforms



EMPro Project Setup for EMI Calculation



Selected Data Signals, Strobe, clocks ,Power nets and Grounds and 'Copy to design' in new ADS layout

↓

Simplify Ground and remove undesired shapes and vias

↓

Export design from ADS to EMPro, cross check ports and perform FDTD simulation

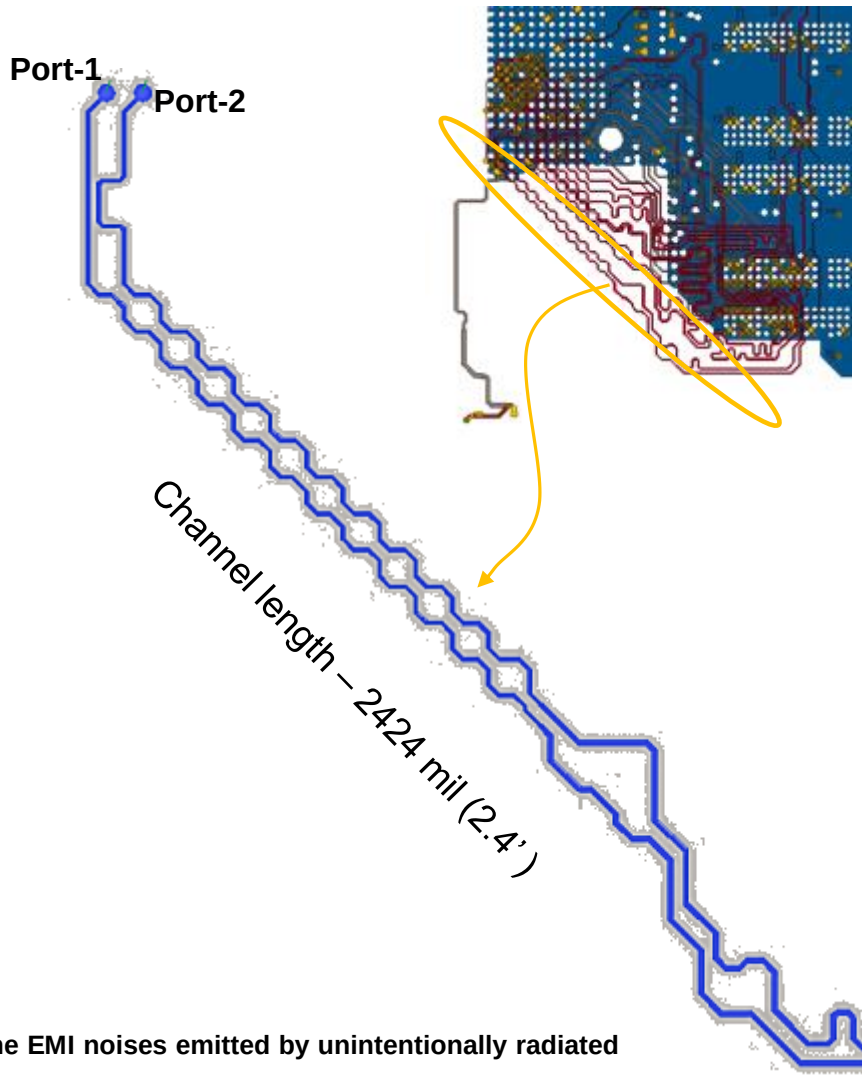
↓

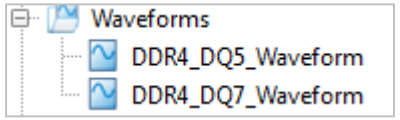
EMI Simulation Run in EMPro

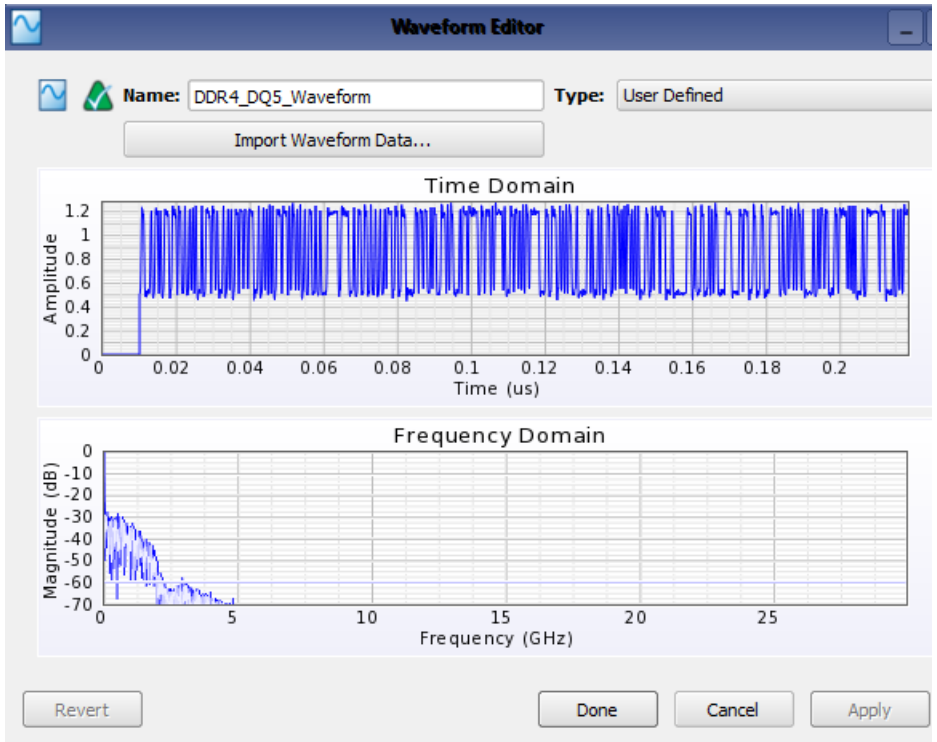
↓

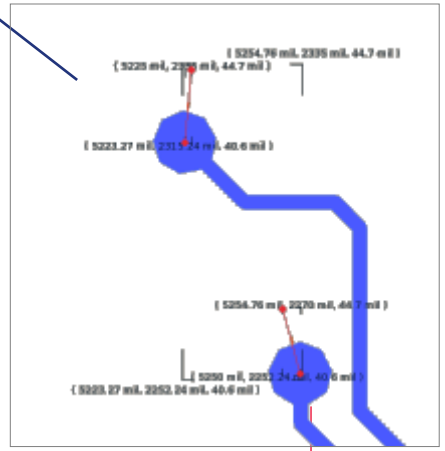
EMI Compliance

Data Signal DQ5 & DQ7







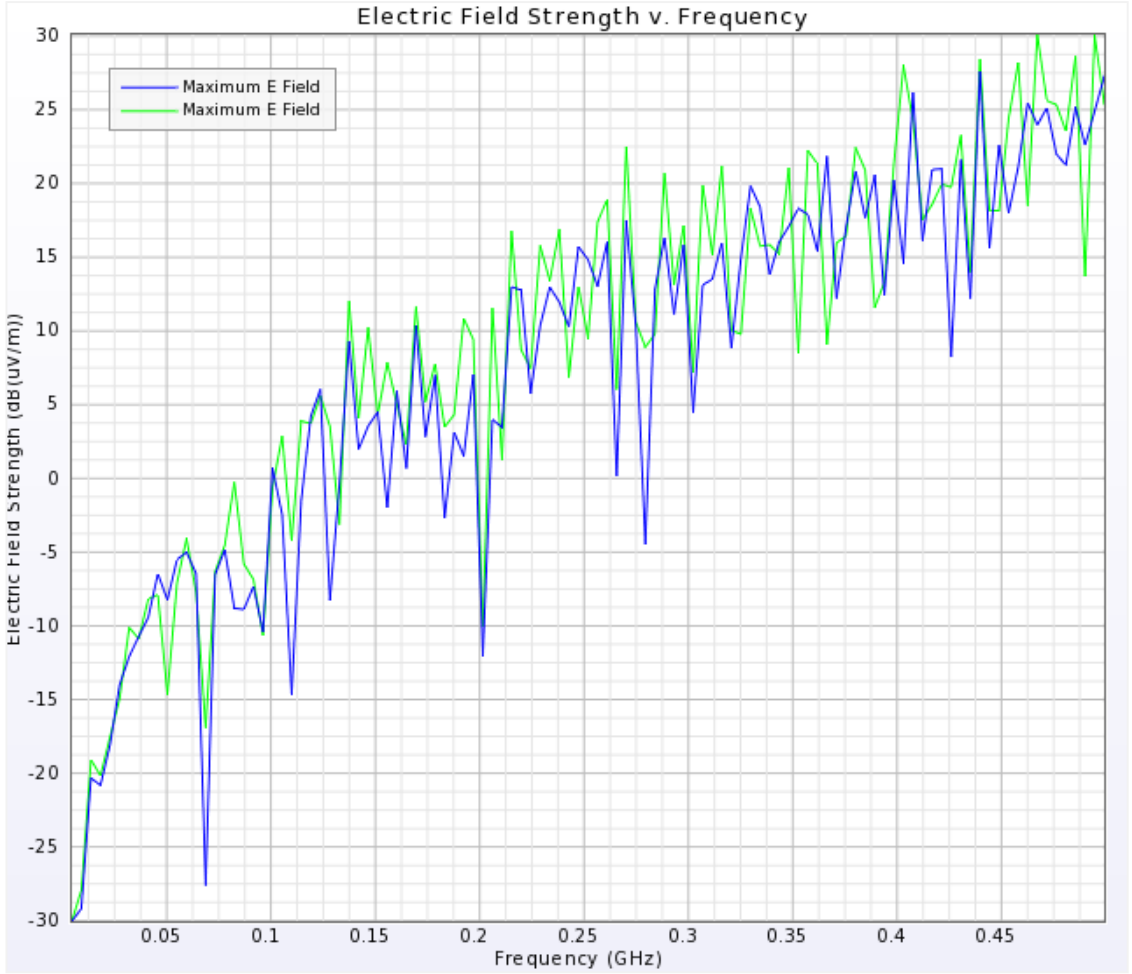


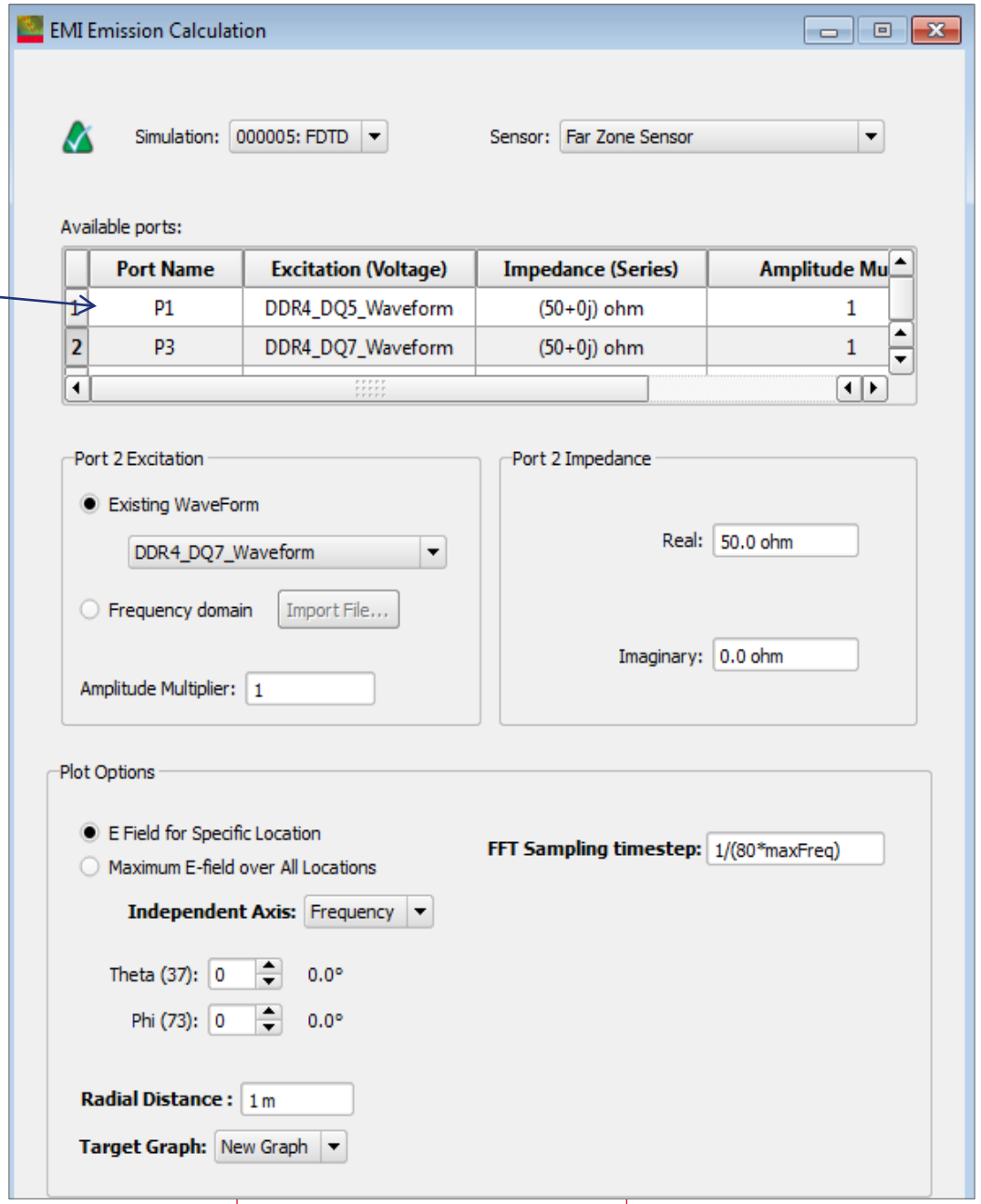
ADS DDR4 Power Aware SI generated waveform is imported in EMPro for EMI Analysis

The EMI noises emitted by unintentionally radiated interference sources (that may be data line also) may severely impact the performance of devices, and thus result in the severe performance degradation of digital signals.

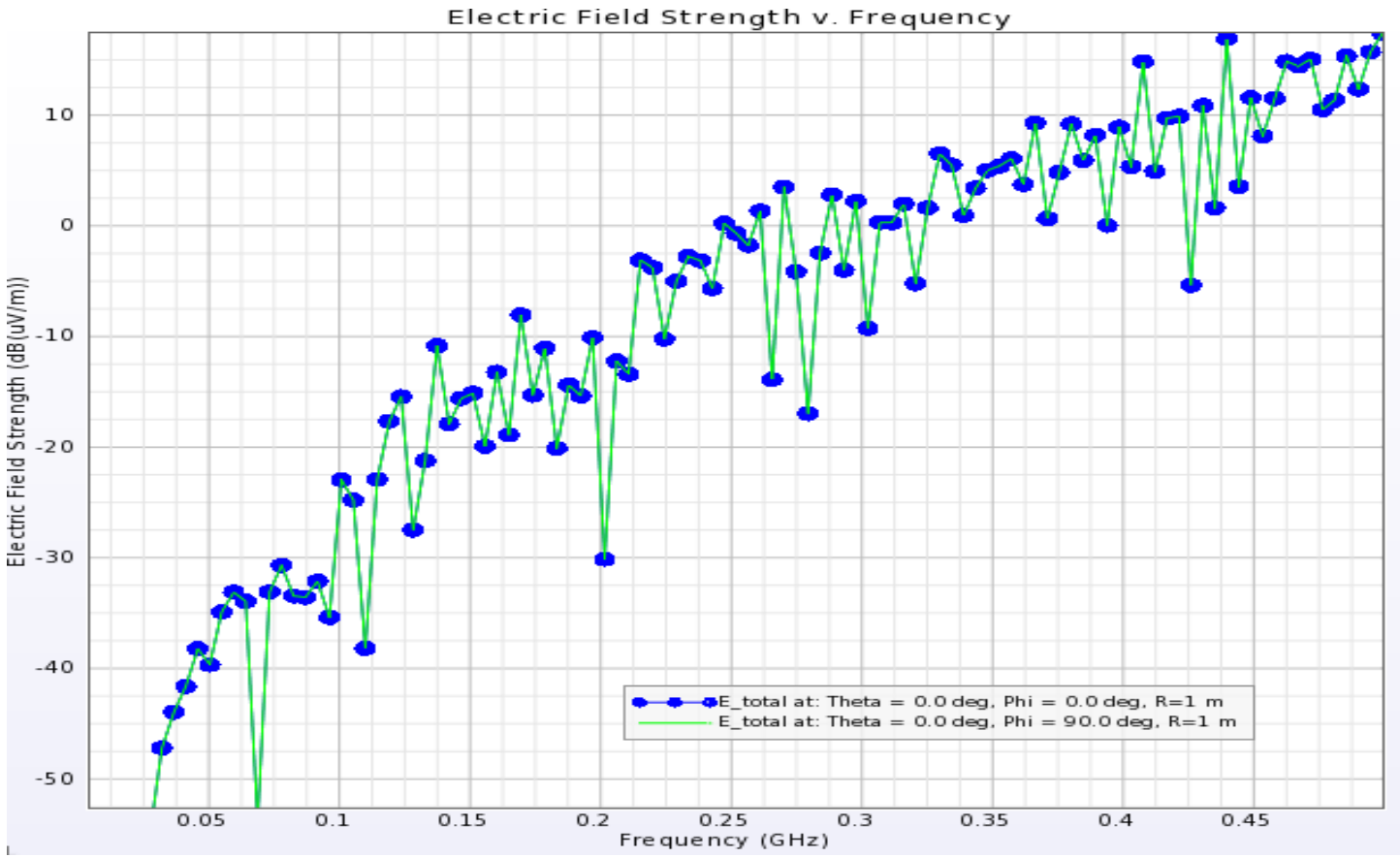
EMI Analysis Result

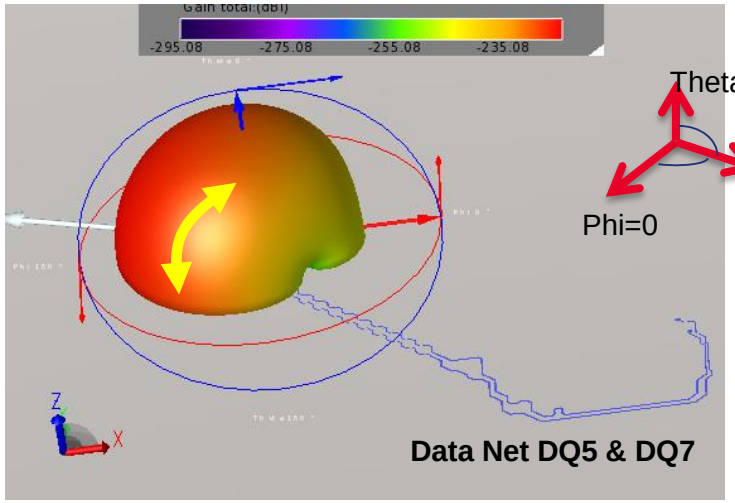
Use imported waveforms for different ports in EMI Analysis Wizard.





EMI : Electric Field vs. Theta

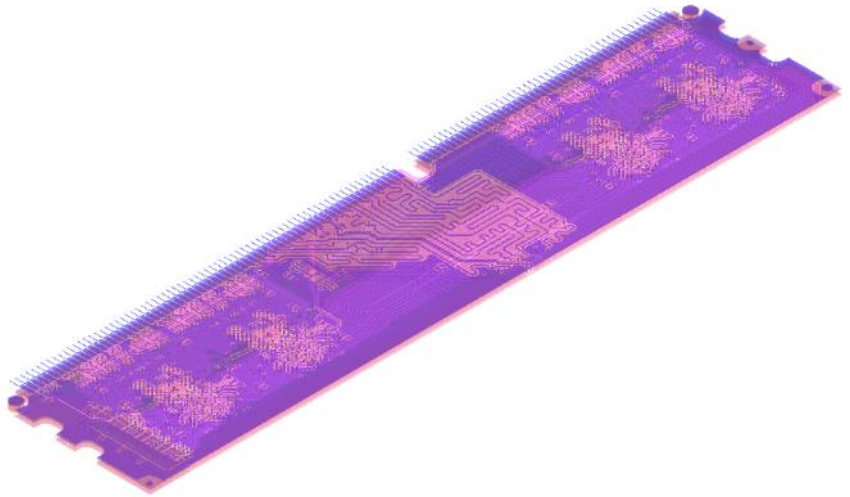




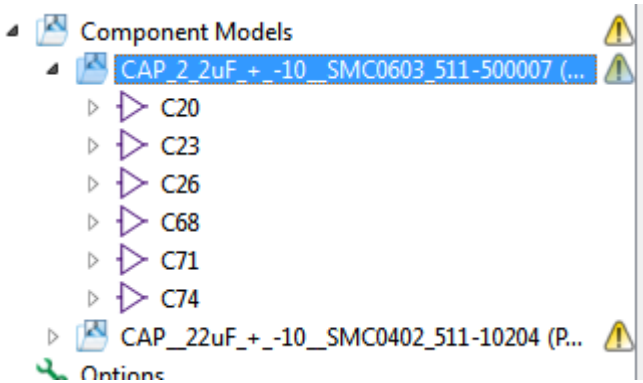
Along the channel : Phi-0, Theta- 0 & 90 degree

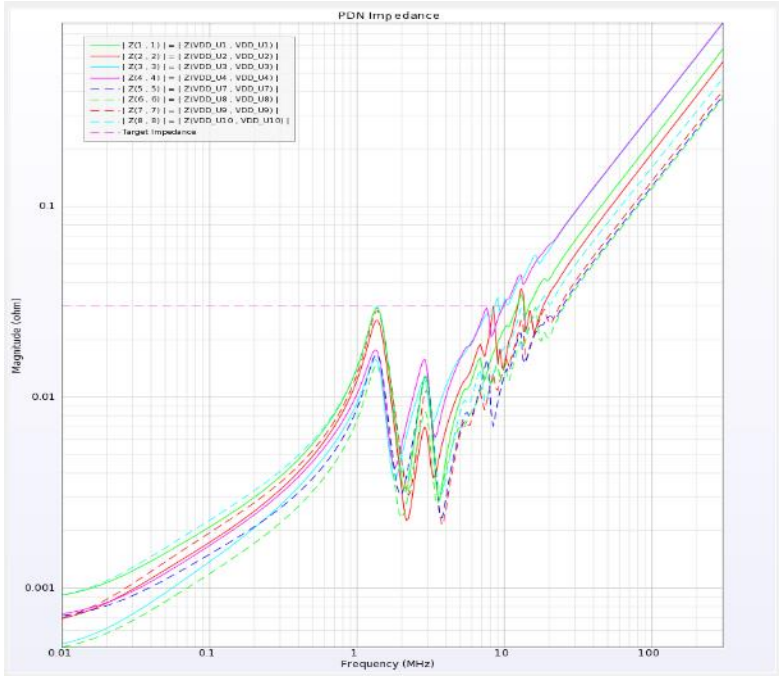
PIPro: PDN Impedance Analysis

Hands-on Workshop Available: DDR3 Memory card



- Analyze the PDN Impedance of a DDR3 memory card
- You will learn
  - How to add the relevant decaps in the analysis and assign models
  - How to run a PI-AC analysis
  - View the PDN Impedance and add a target impedance line
- Lab instructions in a Word document





KEYSIGHT TECHNOLOGIES

Decap Optimization Strategies

Decap Optimization

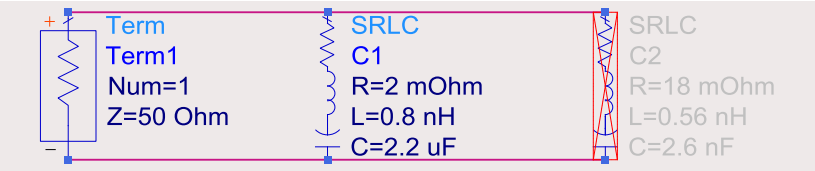
Combining Capacitors in Parallel

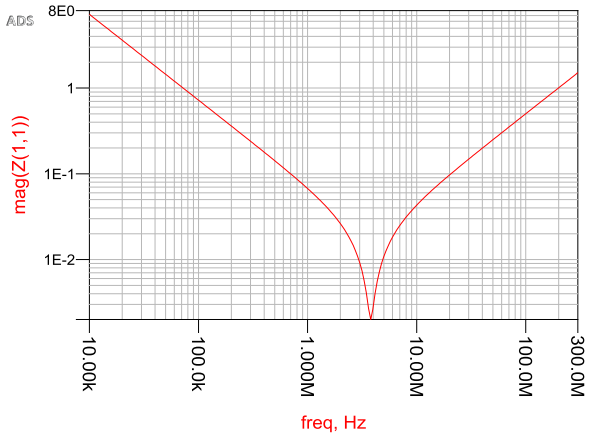
- When multiple, identical capacitors are connected in parallel, assuming the capacitors are independent and their currents do not overlap, it's the entire impedance profile that scales lower.
- When the capacitors have a different value of capacitance or ESL, the behavior is not so simple.
  - An example of two different capacitors (C1 > C2) illustrates it introduces a peak in the impedance, called the parallel resonant peak, which occurs at the parallel resonant frequency (PRF).

Decap Optimization

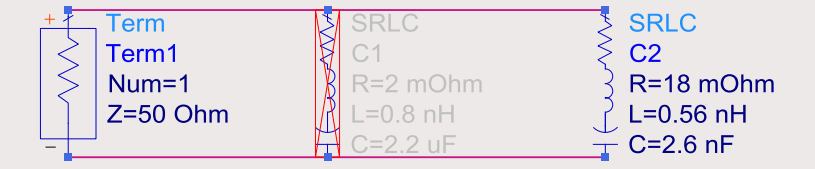
The parallel resonance peak (aka anti-resonance peak)

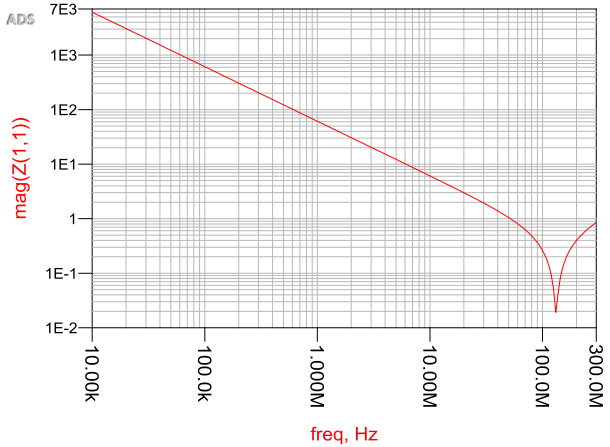
Large C1

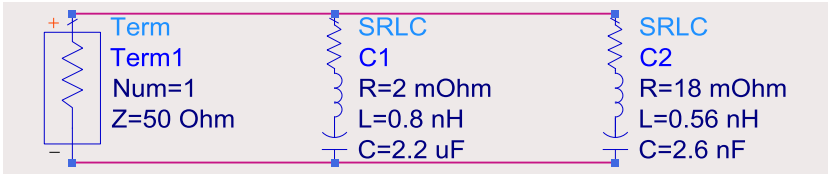


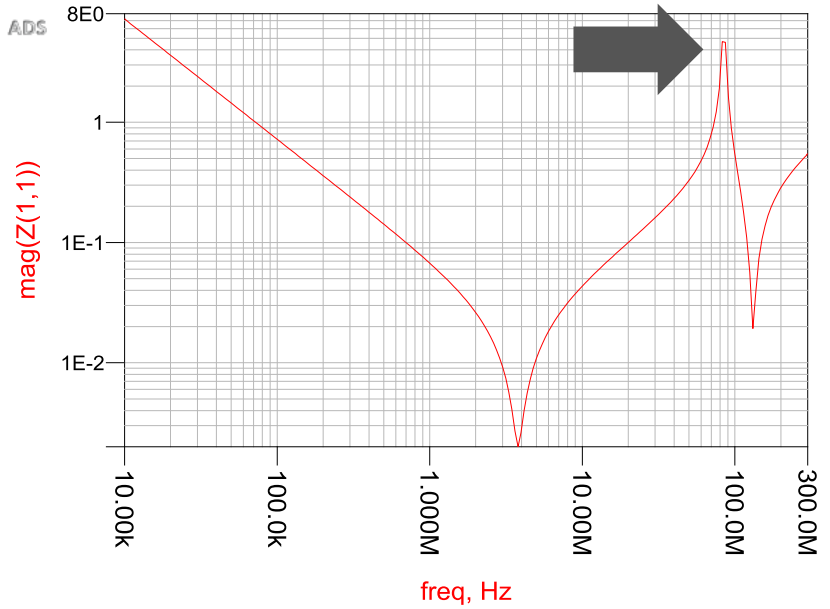


Small C2









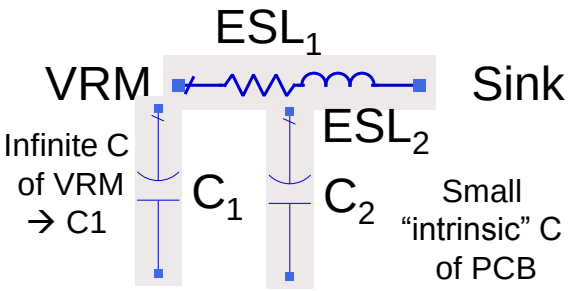
Decap Optimization

Engineering a reduction in the peak impedance

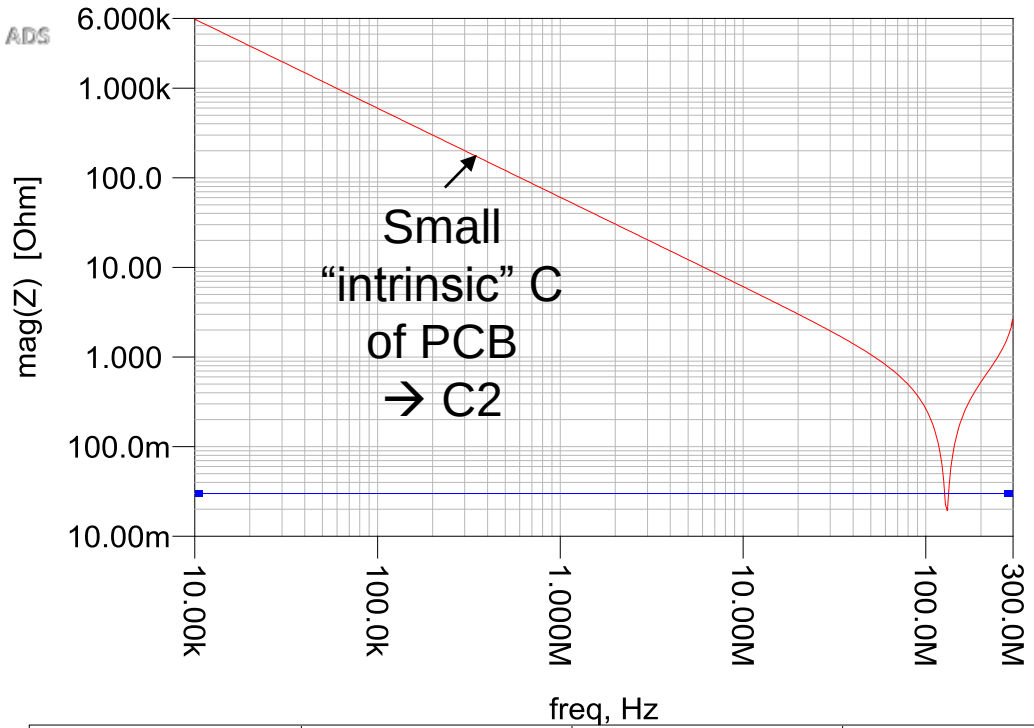
– Important ways:

- Increase the ESR of both capacitors → use more smaller decaps → not cost effective
- Increase the capacitance of the smaller capacitor
- Reduce the ESL of the larger capacitor

Decap Analysis for DDR3

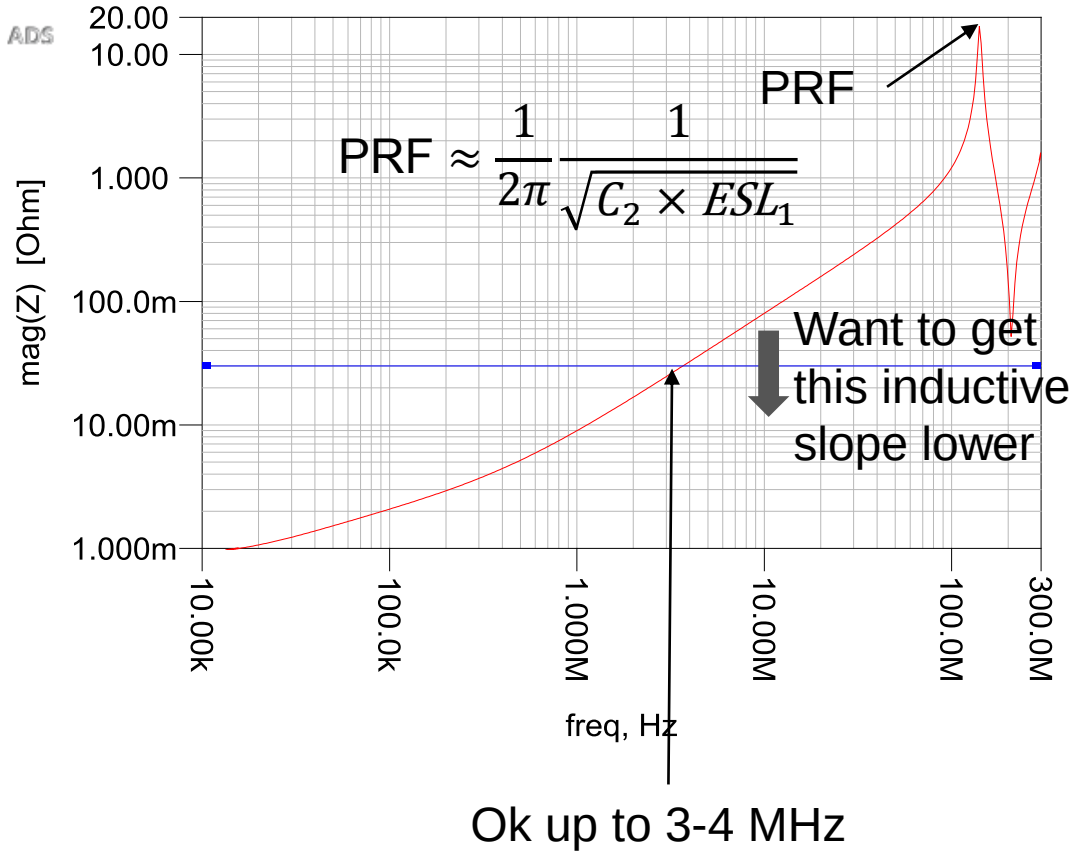


No Decaps, VRM Open



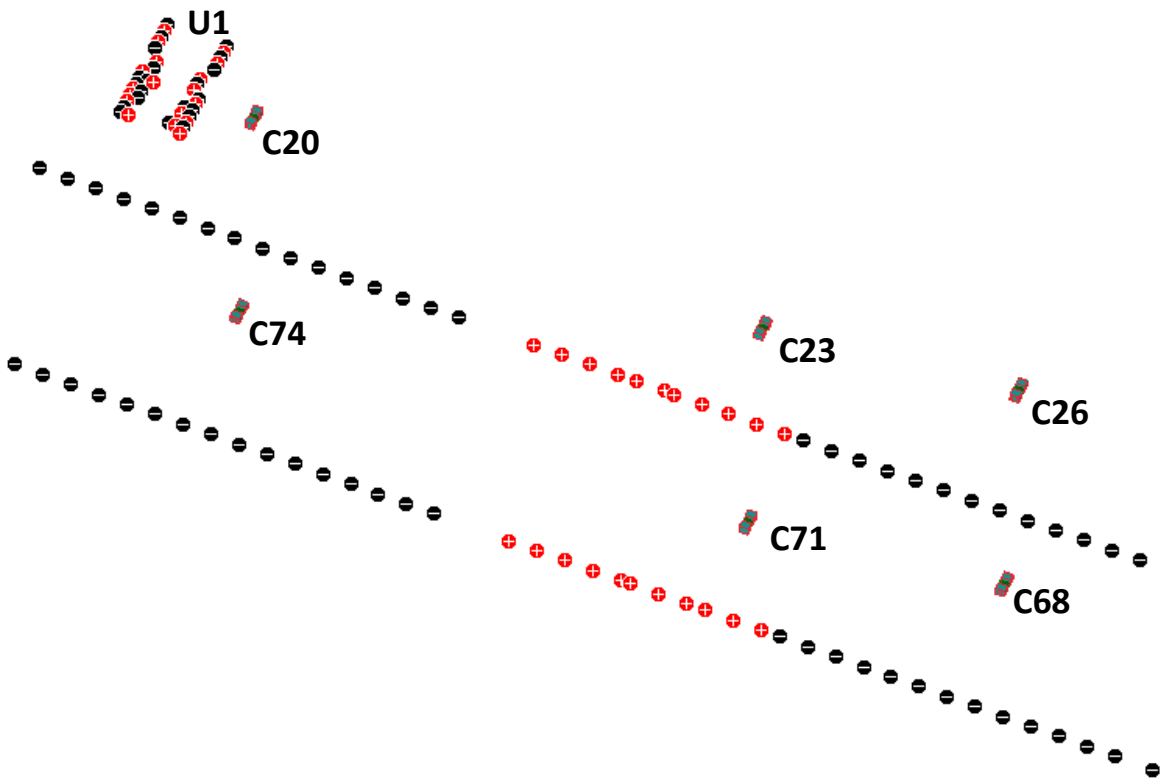
C	ESL	ESR	SRF
2.704E-9	5.457E-10	0.019	1.310E8

No Decaps, VRM Closed

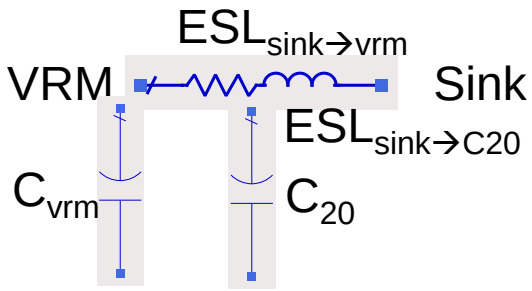


Decap Optimization

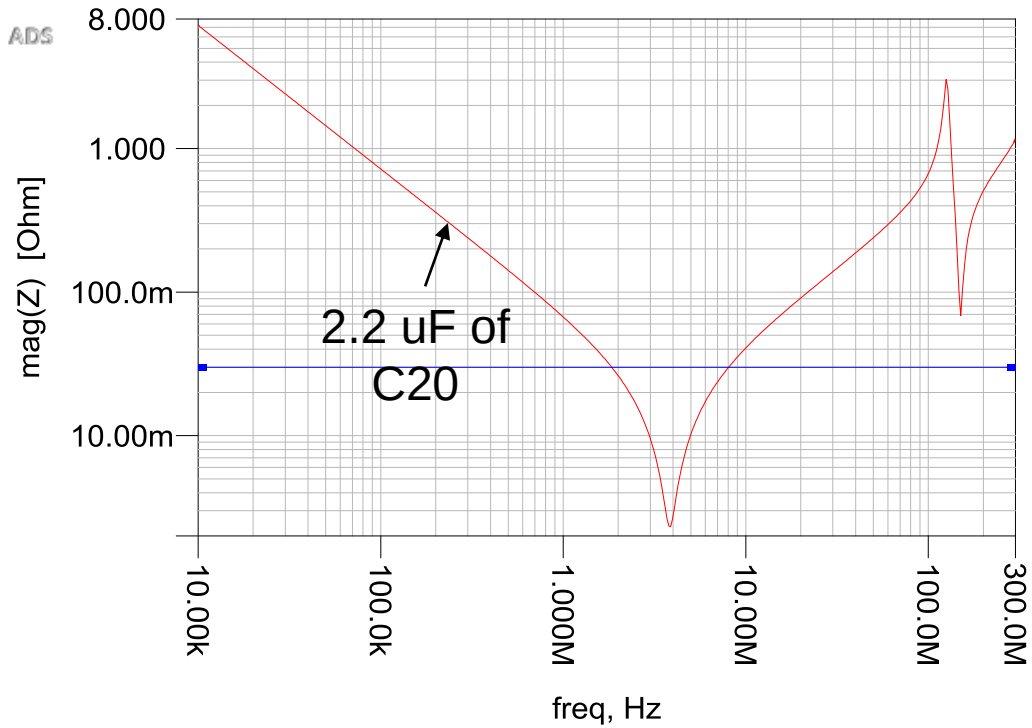
Location of the six 0.22 uF Capacitors



Decap Optimization

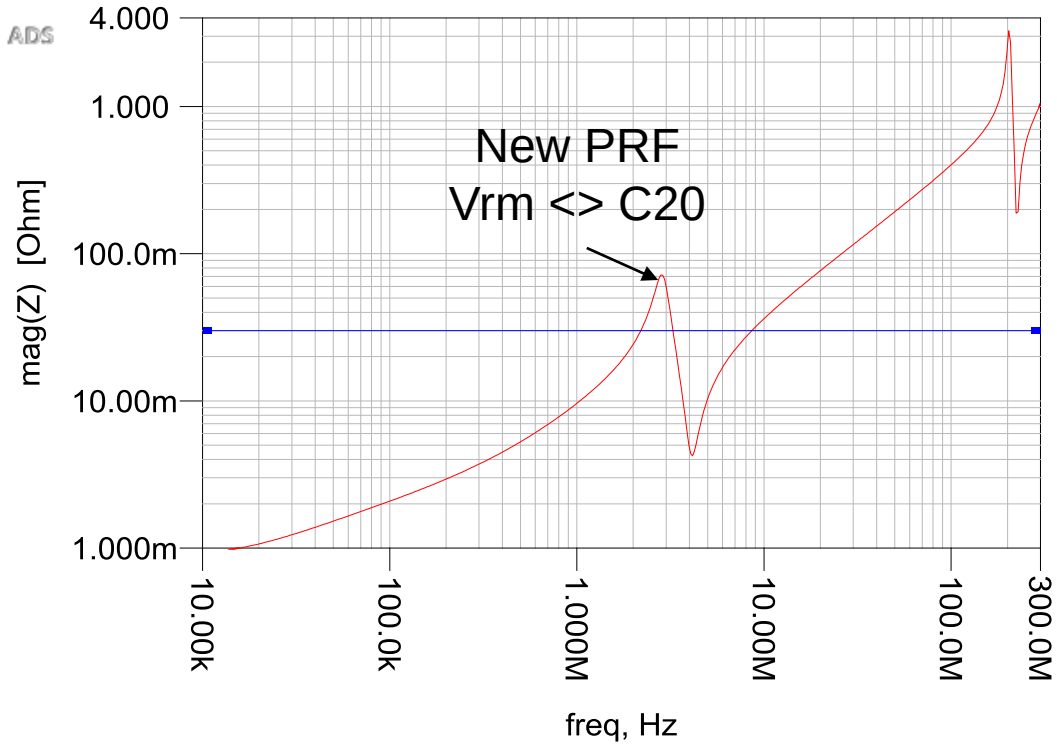


C20 Decap, VRM Open



C	ESL	ESR	SRF
2.203E-6	7.656E-10	0.002	3.876E6

C20 Decap, VRM Closed



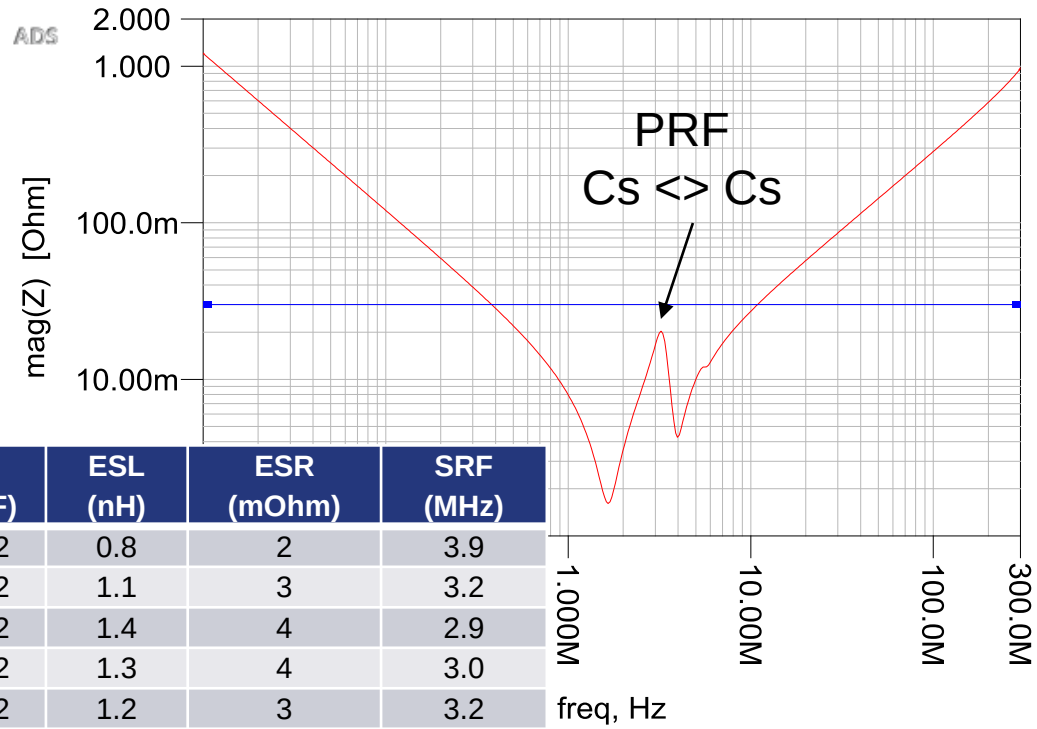
Ok up to 8-9 MHz now but we introduced a parallel resonance impedance peak…

Decap Optimization

Important ways of engineering a reduction in the peak impedance:

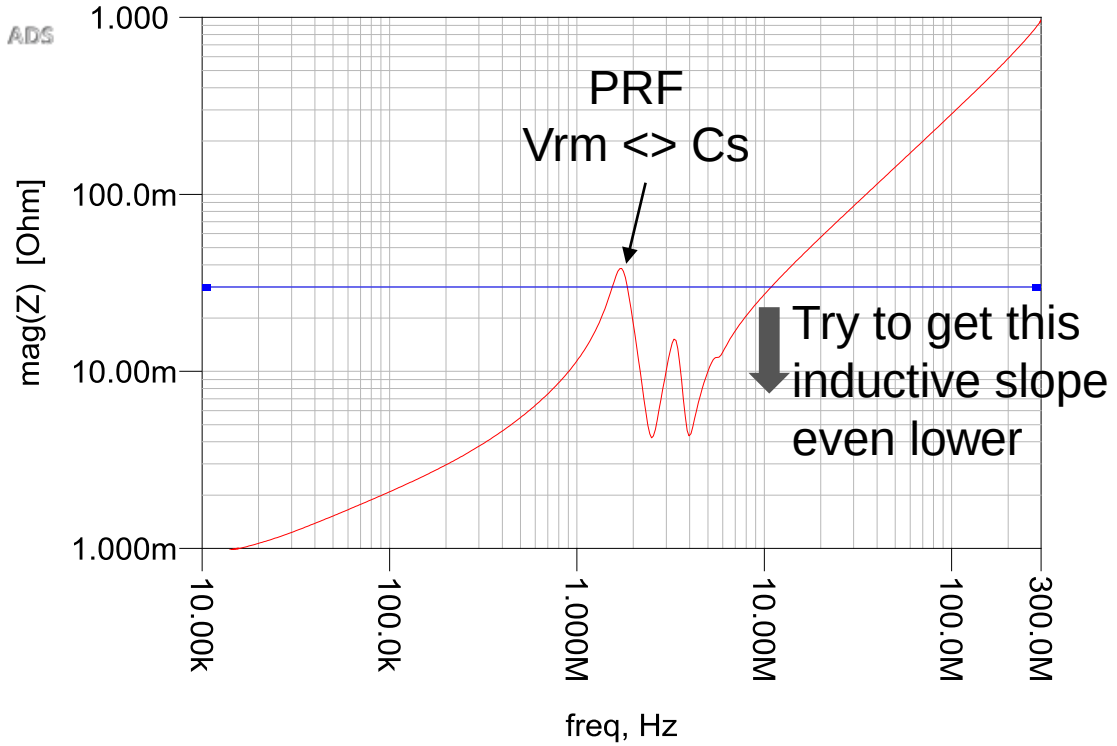
- Reduce the ESL of the larger capacitor → ~~Wider rails, less vias~~
- **Increase the capacitance of the smaller capacitor** → Add 5 more!
- Increase the ESR of both capacitors → ~~Often not cost effective~~

Six 2.2 uF Decaps, VRM Open



ID	C (uF)	ESL (nH)	ESR (mOhm)	SRF (MHz)
C20	2.2	0.8	2	3.9
C23	2.2	1.1	3	3.2
C26	2.2	1.4	4	2.9
C68	2.2	1.3	4	3.0
C71	2.2	1.2	3	3.2
C74	2.2	0.6	2	4.2

Six 2.2 uF Decaps, VRM Closed

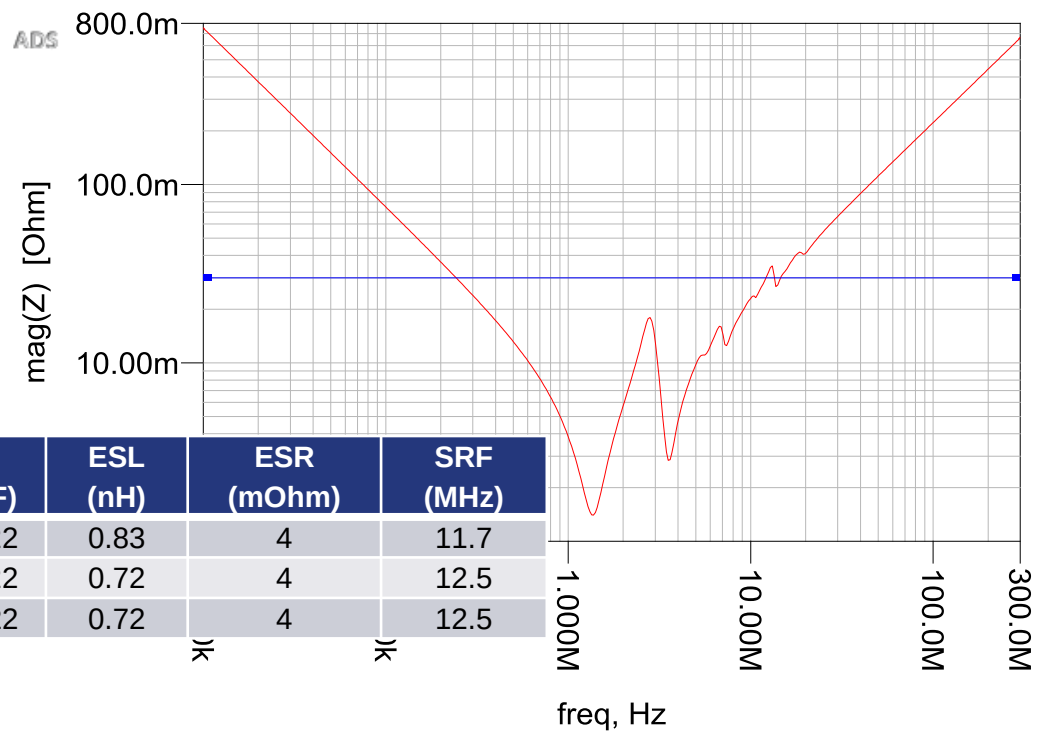


Almost ok up to 10 MHz. The little extra C still needed will come from the ones need to improve higher frequencies…

Decap Optimization

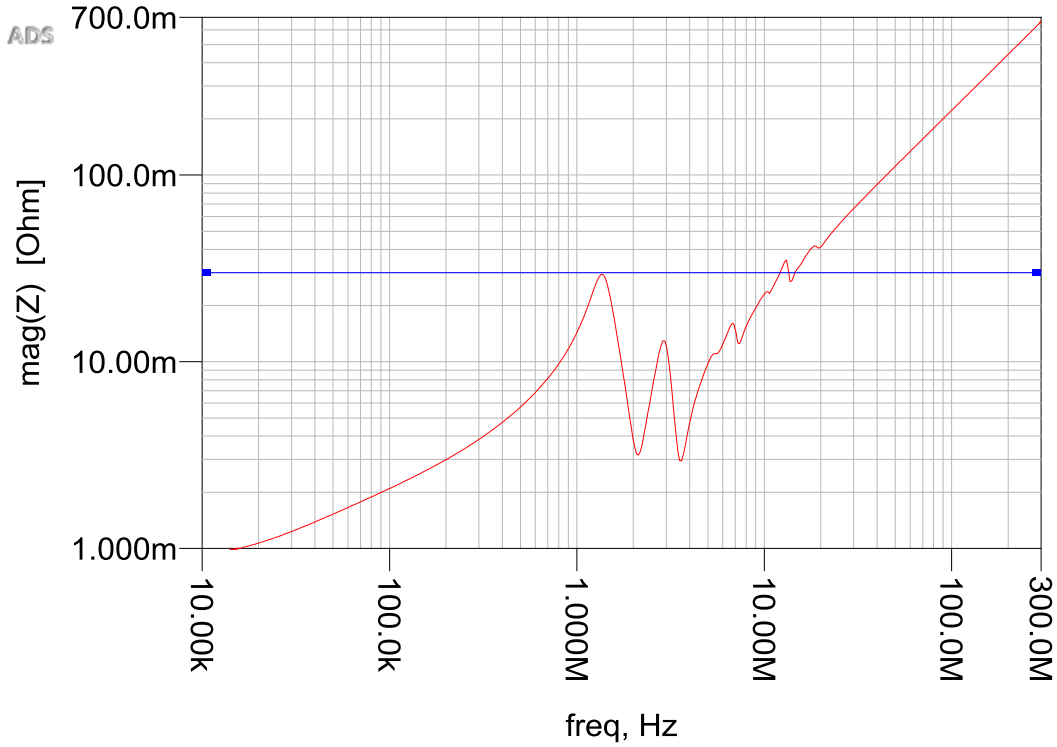
→ Enable all 74 0.22 uF Capacitors.

All Decaps, VRM Open



ID	C (uF)	ESL (nH)	ESR (mOhm)	SRF (MHz)
C4	0.22	0.83	4	11.7
C76	0.22	0.72	4	12.5
C84	0.22	0.72	4	12.5

All Decaps, VRM Closed

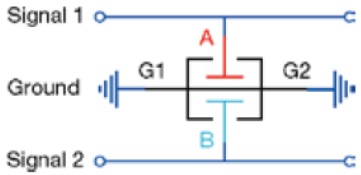


More decaps doesn't help a lot. The ESL limits the improvement…

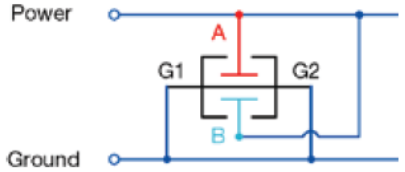
Lowering ESL: X2Y© Filter and Decoupling Capacitors

When every pH counts

EMI Filtering S21
Signal-to-Ground

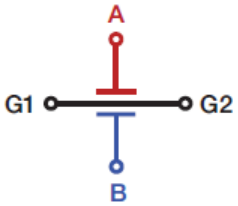


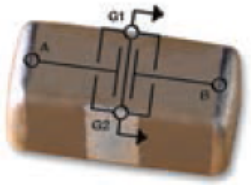
Power Bypass S21
Power-to-Ground



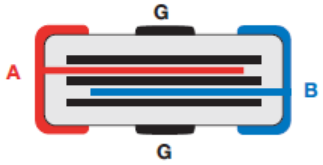
Labeled capacitance values below follow the P/N order code (single Y cap value)
Effective capacitance measured in Circuit 2 is 2X of the labled single Y cap value.

Equivalent Circuits

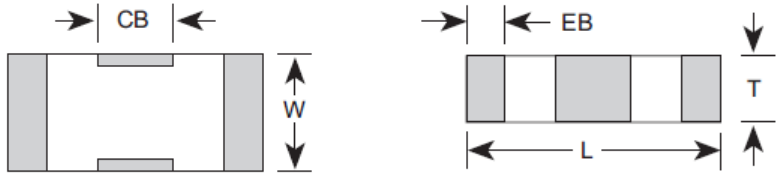


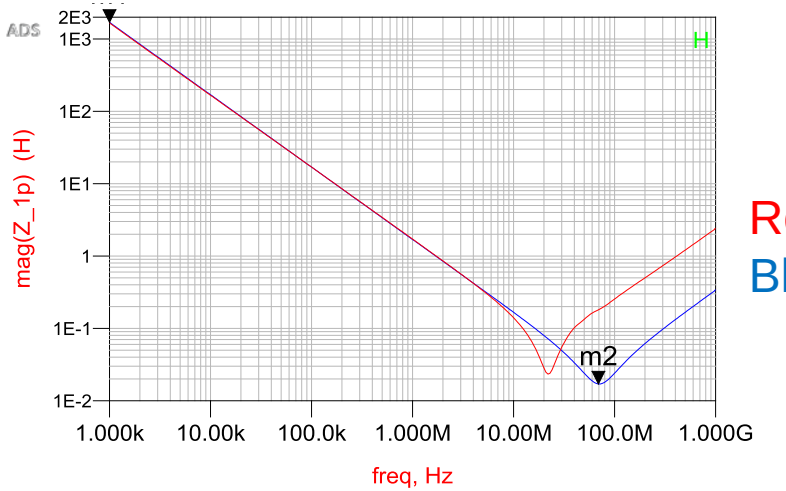


Cross-sectional View



Dimensional View

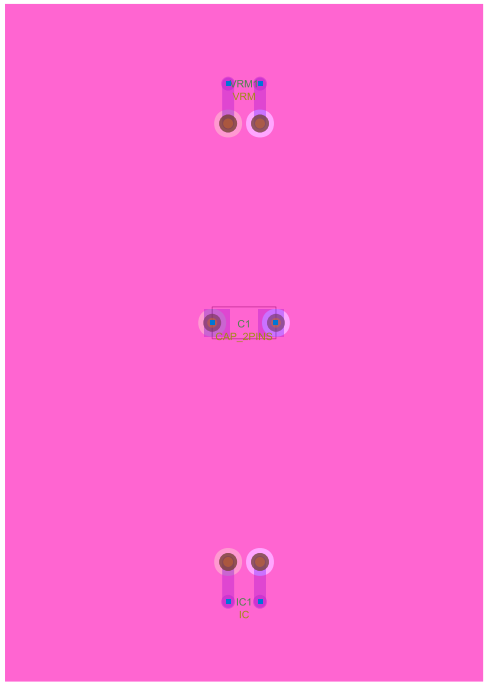




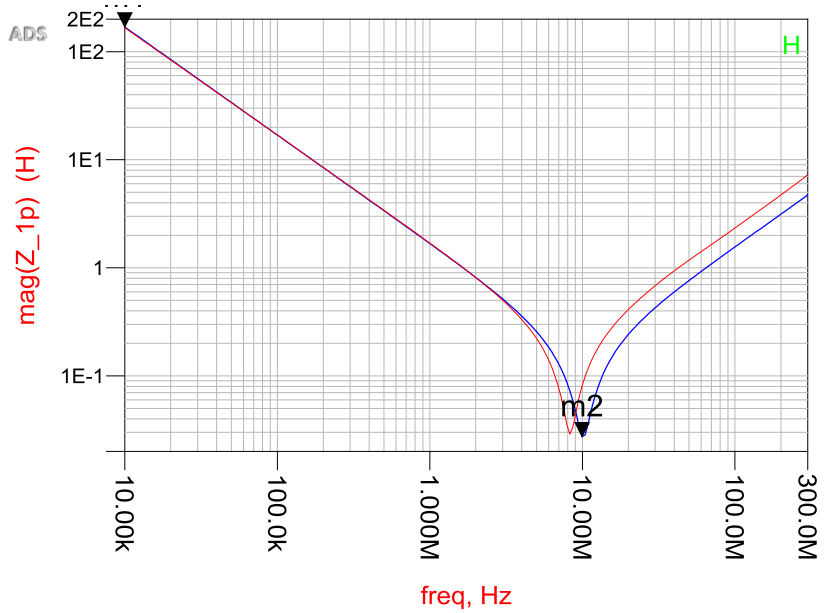
Red: Murata general purpose
Blue: X2Y

Lowering ESL: impact of the mounting

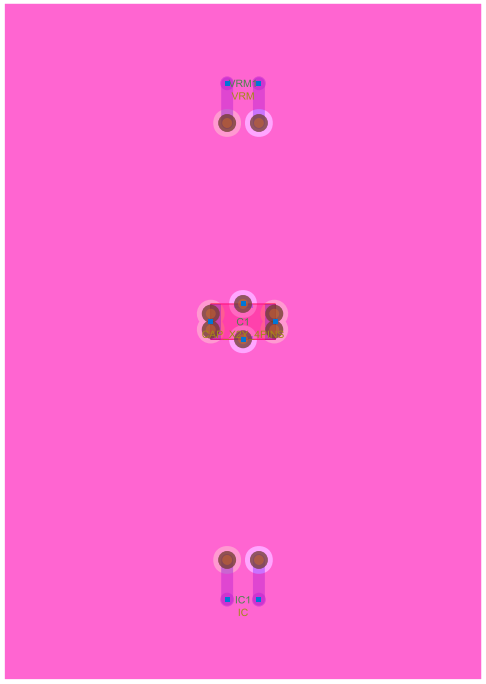
Murata General Purpose 0603



Red: Murata general purpose
Blue: X2Y



X2Y 0603



Additional topics…

Power Plane Resonance Analysis

Why doing an PPR analysis?

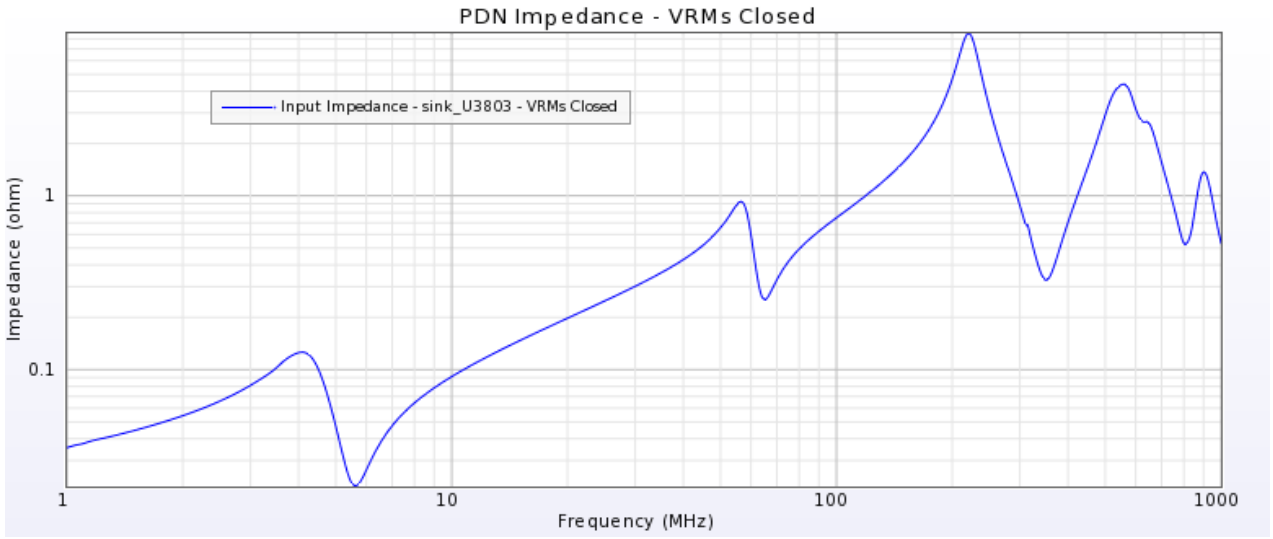
- Resonance frequencies (comparing to AC)
  - Quickly get all resonance frequencies in a range without frequency sweep (AFS in AC can be slow to converge)
  - The resonances are natural resonances (the S parameter from AC simulation show resonances only related to ports (VRMs and sinks))
- Surface current and fields
  - PI: suggestions of decap placements at high resonance fields
  - SI: avoid routing of signal lines close to high resonance fields, if the resonance frequency is close to the signal rate and its harmonics.

Power Plane Resonance Analysis

Correlation with AC analysis

Customer design: 38,469 vias, 16 decaps with from C = 5.6 pF to 22 uF

	Eigenfrequency	Q value
1.	5.09128 MHz	3.990776e+000
2.	57.7227 MHz	7.814798e+000
3.	63.0138 MHz	8.871677e+000
4.	183.883 MHz	5.104642e+000
5.	209.91 MHz	6.553459e+000

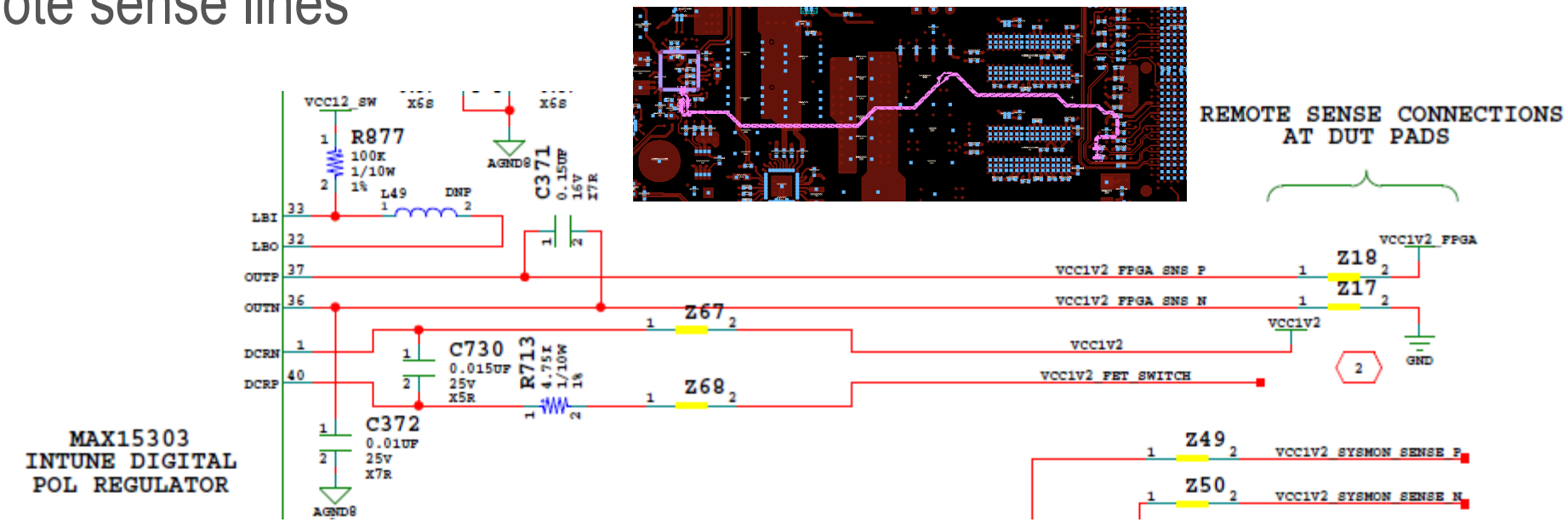


PPR: 10 GB, 23 min

PI-AC: 9 GB, 60 min

Additional Topics

Remote sense lines



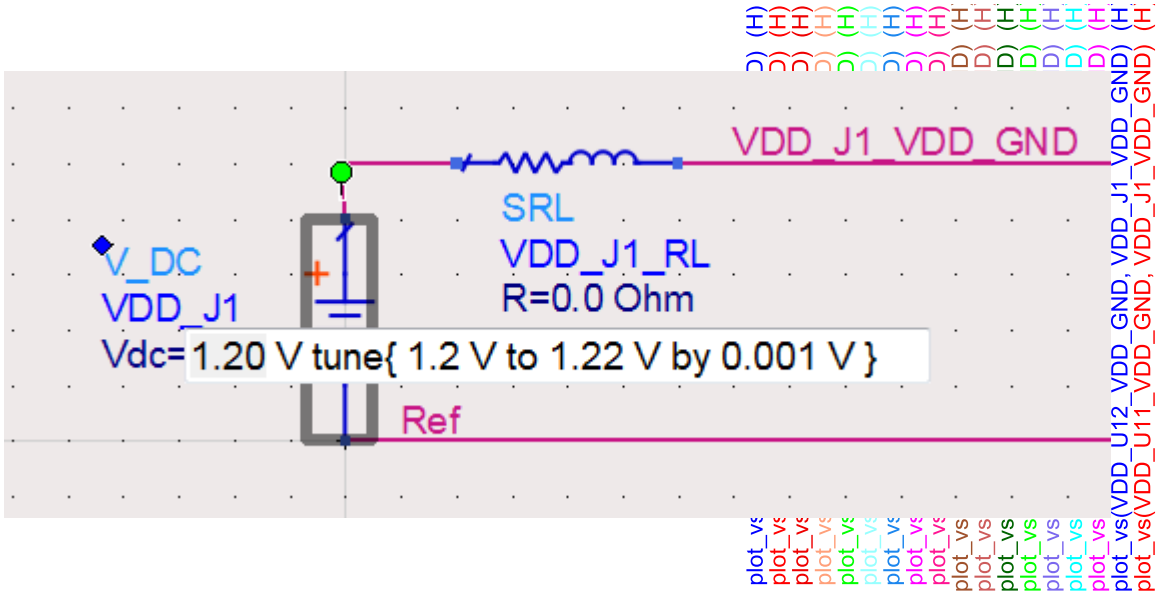
In case there are multiple sinks on the power rail, some nearby, some further away from the VRM, the VRM may remote sense the IR drop at a ‘representative’ location and use that feedback to adjust its output voltage level.

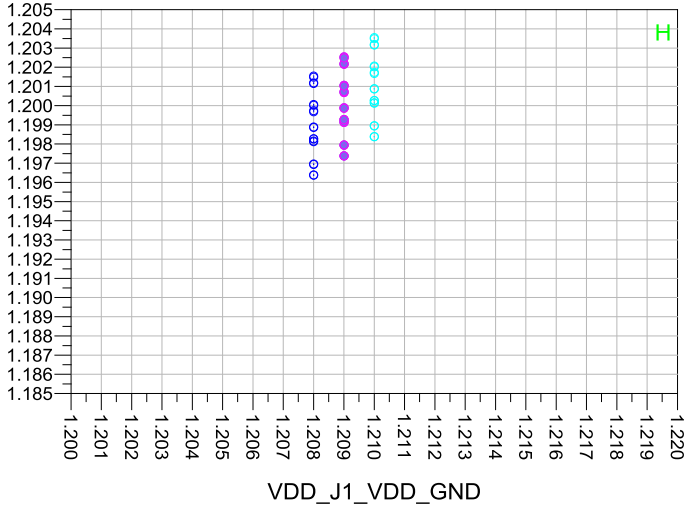
– How to select that location?

– How to verify that nearby devices aren’t overbiased?

Additional Topics

Remote sense lines





– Run a PI-DC analysis and generate a test bench schematic.

– Tune the VRM voltage so that the voltages delivered at the sinks fall within the minimum and maximum specification.

  - Select the representative sink to serve as remote sense location
  - Alternatively, use the voltage distribution plot to decide on the location. Insert top level pins and define a virtual sink (not drawing a relevant current)