

创龙 TMS320C665x 开发板快速体验

Revision History

DraftDate	Revision No.	Description
2018/04/02	V1.1	1.排版修改及勘误。
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2.1 创龙 TMS320C665x NOR FLASH 启动测试

将开发板的拨码开关拨到 IBL NOR 模式，这个档位是 IBL NOR FLASH 启动模式，是二级启动程序。开发板上电后，串口终端会打印信息如下图：

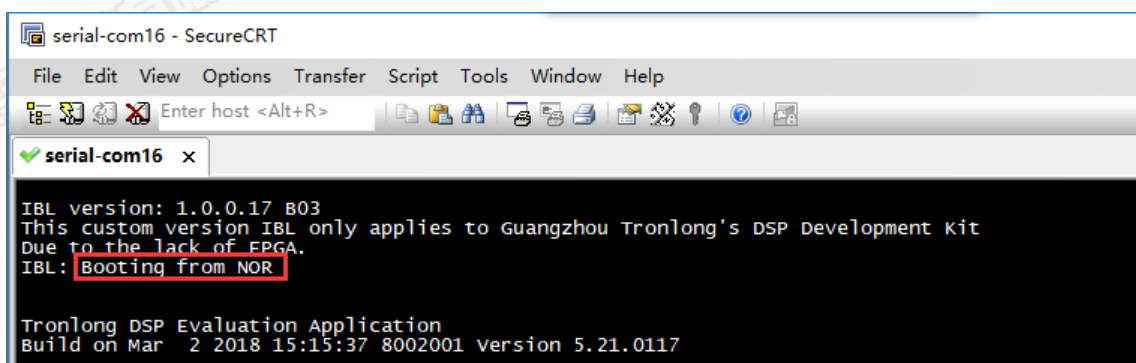


图 6

2.1.1 创龙 TMS320C665x 快速测试

快速测试可以测试开发板绝大部分功能，执行以下命令进行快速测试：

Tronlong > alltest

串口终端会打印硬件信息、硬件测试以及软件测试，如下图所示：

```
Tronlong > alltest
[ 0 0001 0000000000000001]
CPU C665x 1000MHz
DDR3 1333MT/s
Temperature 34
----- Hardware -----
LED Blinking... Tronlong > Finished.
DDR3 Testing...
- Start Address 0x80102F50
- Start Address 0x82102F50
Finished 0.
SRI0 Loopback Testing...
SRI0 initializing...
Port is ok
Send data to Device
Source Device ID 0x0001 Address = 0x80102F50
Destination Device ID 0x0001 Address = 0x80103350
Waiting for LSU to be available.....
Transfer finished
0 data mismatch.
Flash Read/write Testing...
- EEPROM passed
- Nor passed
- Nand passed
----- Software -----
x00afµ+c'c.C0E0D0Uxi0A0A0Ux'i-f-D0AU=aE0EY%Y%o'0'fz%jf
Matrix Testing...
Convert RGB24 Image to Gray Image
Execution Time 7587.2020000000us
FFT Testing...
- Fixed Point
Formula:y=2+3cos(2pi*50t-(30/180)pi)+1.5cos(2pi*75t+(90/180)pi)
16 Point FFT Execution Time is 0.0000000 us IFFT Execution Time is 0.0000000 us
32 Point FFT Execution Time is 0.3780000 us IFFT Execution Time is 0.2630000 us
64 Point FFT Execution Time is 0.7180000 us IFFT Execution Time is 0.4250000 us
128 Point FFT Execution Time is 0.8170000 us IFFT Execution Time is 0.4880000 us
256 Point FFT Execution Time is 1.4060000 us IFFT Execution Time is 1.1710000 us
512 Point FFT Execution Time is 2.4089999 us IFFT Execution Time is 2.0950000 us
1024 Point FFT Execution Time is 5.7919998 us IFFT Execution Time is 5.0050001 us
2048 Point FFT Execution Time is 10.1250000 us IFFT Execution Time is 8.5340004 us
4096 Point FFT Execution Time is 22.4309998 us IFFT Execution Time is 19.8220005 us
8192 Point FFT Execution Time is 41.5270004 us IFFT Execution Time is 35.9500008 us
16384 Point FFT Execution Time is 99.6979980 us IFFT Execution Time is 89.7389984 us
32768 Point FFT Execution Time is 371.7189941 us IFFT Execution Time is 338.7839966 us
65536 Point FFT Execution Time is 1126.7939453 us IFFT Execution Time is 1073.4449463 us
- Floating Point
Formula:y=2+3cos(2pi*50t-(30/180)pi)+1.5cos(2pi*75t+(90/180)pi)
16 Point FFT Execution Time is 0.0000000 us IFFT Execution Time is 0.0000000 us
32 Point FFT Execution Time is 0.7570000 us IFFT Execution Time is 0.5490000 us
64 Point FFT Execution Time is 0.8420000 us IFFT Execution Time is 0.3350000 us
128 Point FFT Execution Time is 1.2860000 us IFFT Execution Time is 0.6510000 us
256 Point FFT Execution Time is 1.9540000 us IFFT Execution Time is 1.4069999 us
512 Point FFT Execution Time is 3.9400001 us IFFT Execution Time is 2.4189999 us
1024 Point FFT Execution Time is 7.8720002 us IFFT Execution Time is 4.9889998 us
2048 Point FFT Execution Time is 15.8900003 us IFFT Execution Time is 11.0769997 us
4096 Point FFT Execution Time is 31.4270000 us IFFT Execution Time is 21.4880009 us
8192 Point FFT Execution Time is 63.4309998 us IFFT Execution Time is 49.7719994 us
16384 Point FFT Execution Time is 132.7669983 us IFFT Execution Time is 117.0039978 us
32768 Point FFT Execution Time is 438.5979919 us IFFT Execution Time is 421.1520081 us
65536 Point FFT Execution Time is 1537.9670410 us IFFT Execution Time is 1548.1280518 us
131072 Point FFT Execution Time is 5965.5961914 us IFFT Execution Time is 6014.1582031 us
262144 Point FFT Execution Time is 12527.0341797 us IFFT Execution Time is 15659.4736328 us
```

图 7

测试现象：

表 1

测试项目	现象	备注
核心板 LED	核心板两个 LED 闪烁，一个呼吸灯继续呼吸	
底板 LED	底板 LED 闪烁	根据开发板型号不同，LED 数目不同
底板定时器 LED	底板 LED 闪烁	
DDR3	随机测试 DDR3 内存区域，并打印测试误码	
温度	输出当前温度传感器温度值	
存储器	测试指定区域 EEPROM、NOR 以及 NAND 存储器	测试通过显示 Passed
算法性能测试	FFT 不同点数测试	仅供参考
SRIO	SRIO 回环测试	测试通过显示 Port is ok

2.1.2 创龙 TMS320C665x 进阶测试

进阶测试条目为更加灵活的测试命令或者不方便通过统一测试命令进行测试的功能。

执行以下指令查看所支持的命令：

Tronlong > help

```
Tronlong > help
Available commands
-----
h - Display list of commands
help - Display list of commands
clear - Clear the display
ndk - Config the NDK stack
temp - Get the temperature sensor value
rmem - Read any memory data including register
wmem - Write data to any memory including register
fan - CPU Fan control
led - LED control
sriotest - SRIO communication test
pcietest - PCIe communication test
cpuinfo - display CPU information
flashinfo - EEPROM / Nor Flash / NAND Flash information
flashtest - EEPROM / Nor Flash / NAND Flash test
meminfo - System heap information
memtest - Internal memory and DDR3 memory test
matrixtest - Matrix-Vector Multiplication test
ffttest - FFT Real number test
fft2test - FFT Real number test
nand
mkfs
ls
mkdir
pwd
rm
cd
cat
ram:
nand:
fatfstest
fpga12c
fpgaemif
fpgaupp
fpgasrio
fpgaprogram
tftp
time
settime
synctime
restart
alltest
camlink
```

图 8

(1) 网络测试

网络功能需要额外初始化才能使用，支持 DHCP 自动获取 IP 方式（需要连接到启用了 DHCP 服务的网络环境，典型情况是网络中存在路由器并启用 DHCP 服务）。默认使用网口 1。

➤ 动态获取 IP

执行以下指令：

```
Tronlong > ndk dhcp
```

```
Tronlong > ndk dhcp
parameter: dhcp
Service Status:   DHCP:   Enabled:   : 000
Service Status:   Telnet:  Enabled:   : 000
Service Status:   HTTP:   Enabled:   : 000
Service Status:   DHCP:   Enabled:   Running: 000

Network Added: 192.168.1.162
Link Status: 1000Mb/s Full Duplex
Service Status:   DHCP:   Enabled:   Running: 017
DHCP Server ID:
DHCP SetTronlong > rver 1 = '192.168.1.1'

Router Information:
Router 1 = '192.168.1.1'
```

图 9

网络初始化完成后，会输出开发板 IP 地址。打开 Web 浏览器，输入 IP 地址即可访问内建于 DSP 的 HTTP 服务器提供的 Web 页面，如下图所示：

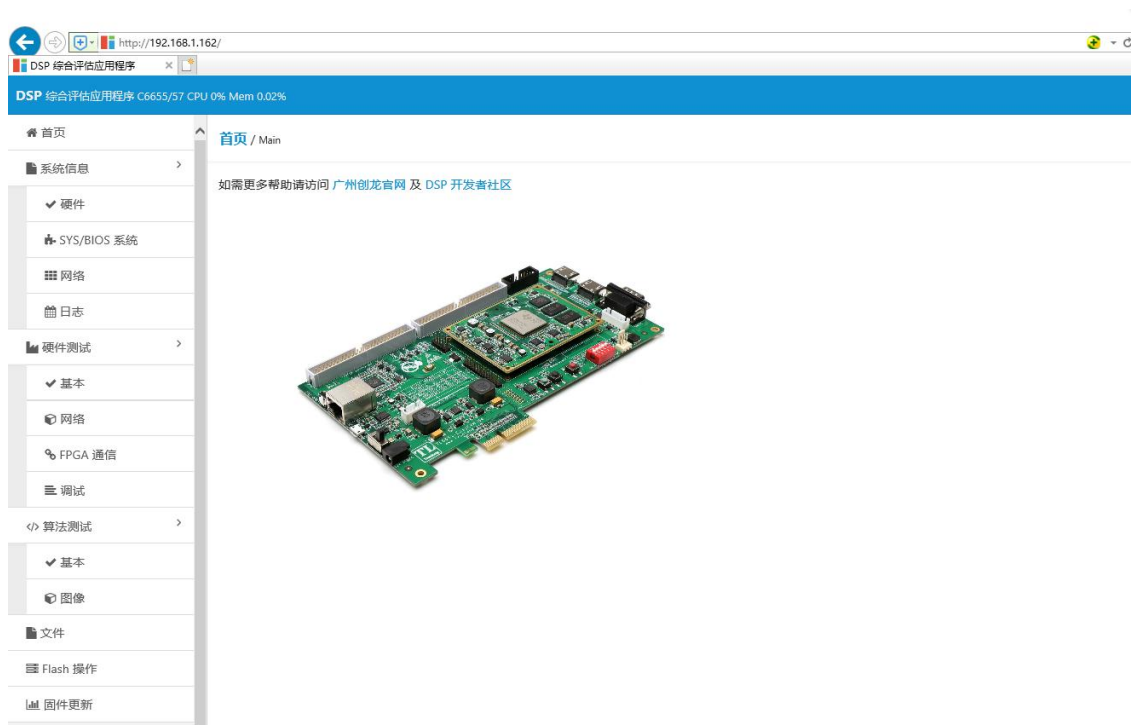


图 10

➤ 静态配置 IP

执行以下指令：

```
Tronlong > ndk static 192.168.0.25 255.255.252.0 192.168.1.1 //192.168.0.25 为配置 IP, 255.255.252.0 为网关, 192.168.1.1 为网段
```


备注：如果配置了动态获取 IP 就不能静态配置 IP 地址，二者不能同时配置。如果先配置了动态获取 IP，需重启开发板后重新执行指令。

```
Tronlong > ndk static 192.168.0.25 255.255.252.0 192.168.1.1
parameter: static
parameter: 192.168.0.25
parameter: 255.255.252.0
parameter: 192.168.1.1

IP Address is set to 192.168.0.25
IP subnet mask is set to 255.255.252.0
IP default gateway is set to 192.168.1.1

Network Added: 192.168.0.25
Service Status:  Telnet:  Enabled:      : 000
Service Status:   HTTP:  Enabled:      : 000
```

图 11

打开 Web 浏览器，输入 IP 地址即可访问内建于 DSP 的 HTTP 服务器提供的 Web 页面，如下图所示：

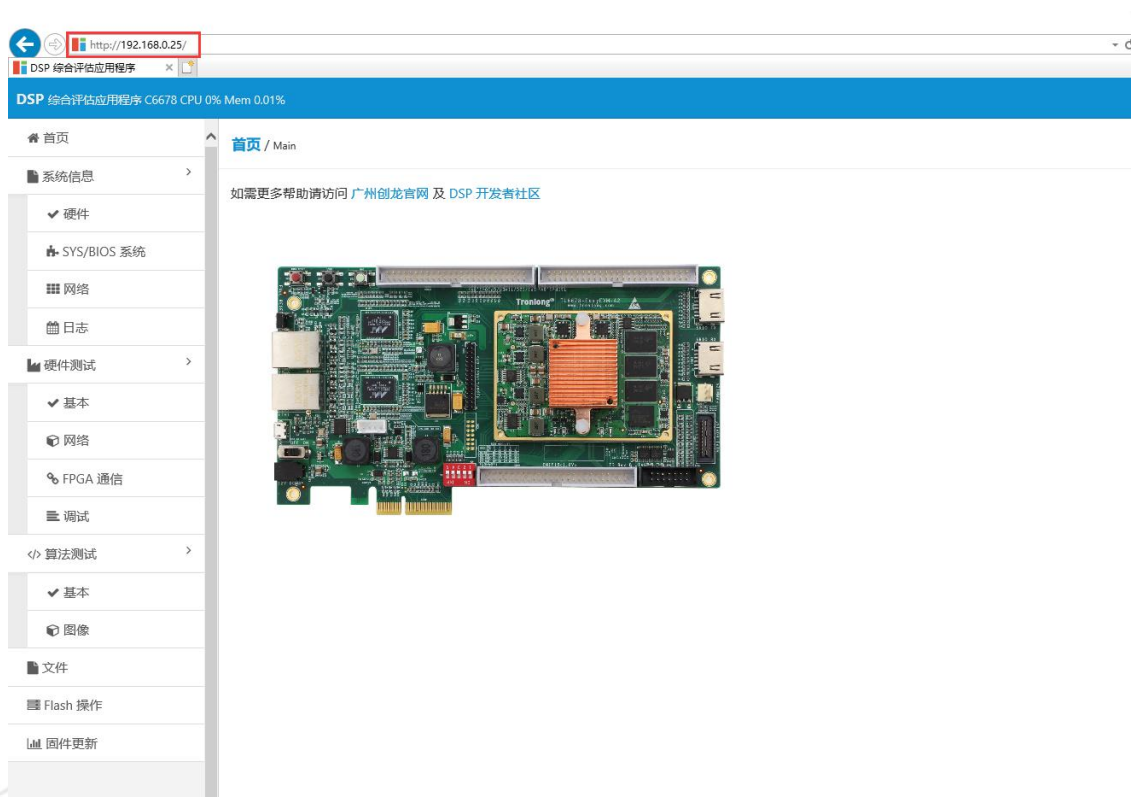
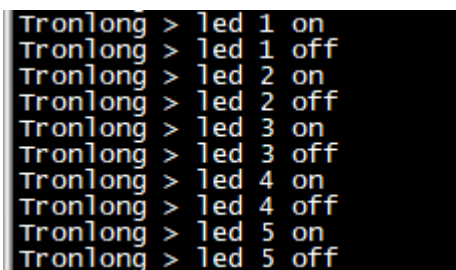


图 12

(2) LED 测试

执行以下命令控制核心板和开发板 LED 的点亮或熄灭，led 1~led 2 分别代表核心板上的 DSP 用户指示灯，led 3~led 5 的分别表示底板上 DSP 用户指示灯。

```
Tronlong > led 1 on
Tronlong > led 1 off
Tronlong > led 2 on
Tronlong > led 2 off
Tronlong > led 3 on
Tronlong > led 3 off
Tronlong > led 4 on
Tronlong > led 4 off
Tronlong > led 5 on
Tronlong > led 5 off
```



```
Tronlong > led 1 on
Tronlong > led 1 off
Tronlong > led 2 on
Tronlong > led 2 off
Tronlong > led 3 on
Tronlong > led 3 off
Tronlong > led 4 on
Tronlong > led 4 off
Tronlong > led 5 on
Tronlong > led 5 off
```

图 13

(3) SRIO 测试

执行以下命令进行 SRIO 回环测试：

```
Tronlong > sriotest loopback 0x80000000 0x90000000 //loopback
```

当前仅支持该参数 0x80000000（任意源地址），0x90000000（目标地址）。目标地址必须为 0x90000000 之后的地址，否则有可能覆盖正常程序

```
Tronlong > sriotest loopback 0x80000000 0x90000000
Start testing srio.....
parameter: loopback
parameter: 0x80000000
parameter: 0x90000000
SRIO initializing...
Tronlong > Port is ok
Send data to Device
    Source Device ID 0x0001 Address = 0x80000000
Destination Device ID 0x0001 Address = 0x90000000
waiting for LSU to be available.....
Transfer finished
0 data mismatch.
```

图 14

"Port is ok"表示接口正常，"0 data mismatch"表示传输无丢失。

(4) FLASH 测试

➤ 输出 FLASH 信息

执行以下命令输出 FLASH 基本信息：

```
Tronlong > flashinfo
```

```
Tronlong > flashinfo
EMIF NAND Device:
Device ID                = 161
Manufacturer ID          = 1
Width                    = 8
Block Count              = 1024
Page Count               = 64
Page Size                = 2048
Spare Size               = 64
Column                   = 2048
Handle                   = 11425
Flag                     = 0
BBOffset                 = 5
Capacity                 = 128 MB
Bad Block Table (only bad block numbers shown):
SPI Nor Device:
Device ID                = 47895
Manufacturer ID          = 32
Width                    = 8
Block Count              = 64
Page Count               = 256
Page Size                = 256
Spare Size               = 0
Column                   = 0
Handle                   = 47894
Flag                     = 0
BBOffset                 = 0
Capacity                 = 4 MB
IIC EEPROM(0x50):
Device ID                = 80
Manufacturer ID          = 1
Width                    = 8
Block Count              = 1
Page Count               = 1
Page Size                = 65536
Spare Size               = 0
Column                   = 0
Handle                   = 80
Flag                     = 0
BBOffset                 = 0
Capacity                 = 64 KB
IIC EEPROM(0x51):
Device ID                = 81
Manufacturer ID          = 1
Width                    = 8
Block Count              = 1
Page Count               = 1
Page Size                = 65536
Spare Size               = 0
Column                   = 0
Handle                   = 81
Flag                     = 0
BBOffset                 = 0
Capacity                 = 64 KB
```

图 15

➤ FLASH 测试

执行以下命令对 FLASH 测试:

Tronlong > flashtest

```
Tronlong > flashtest
Start testing flash memory.....
- EEPROM      passed
- Nor         passed
- Nand        Passed
```

图 16

passed 表示测试通过。

(5) 内存测试

➤ 内存信息

执行以下命令获取内存堆使用情况：

Tronlong > meminfo

```
Tronlong > meminfo
Largest Free Size = 131317472
Total Free Size = 131319648
Total Size = 134217728
```

图 17

➤ 内存测试

执行以下命令进行内存测试：

Tronlong > memtest 0x90000000 0xa0000000 1 //起始地址和结束地址必须为 0x90000000 之后的 DDR3 地址或者其它核心的 L1/L2 RAM，否则有可能覆盖正常程序

```
Tronlong > memtest 0x90000000 0xa0000000 1
- 00 Writing
- 00 Reading & Verifying
- 01 Writing
- 01 Reading & Verifying
Succeeded at 0x90000000 - 0xa0000000
```

图 18

(6) CPU 信息查看

执行以下命令查看 CPU 信息：

Tronlong > cpuinfo

```
Tronlong > cpuinfo
CPU is DSP C665x
CPU Clock is 1000.00 MHz
DDR3 Clock is 1333.33 MT/s
```

图 19

(7) 按键测试

按下用户键，串口终端打印如下信息：

```
Tronlong > [ 1696710686169 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1697051615966 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1697275205317 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1697496606552 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1697726071263 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1697948269070 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1698115414977 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
[ 1698349780790 | KEYSwi @ ../Basic/KEY.C, 52] User key has been pressed
```

图 20

(8) 风扇测试

执行以下命令控制 CPU 风扇的开或关：

Tronlong > fan on

Tronlong > fan off

```
Tronlong > fan on
CPU Fan is on now
Tronlong > fan off
CPU Fan is off now
Tronlong >
```

图 21

(9) PCIe 测试

把两块开发板连接在 TL-PCIe-TC 转接板上，用两条 Micro USB 线分别将两块开发板调试串口接到电脑终端。

执行命令 `pcietest rc` 或 `pcietest ep`，初始化设备为根复合体或端点模式并进入相应测试。

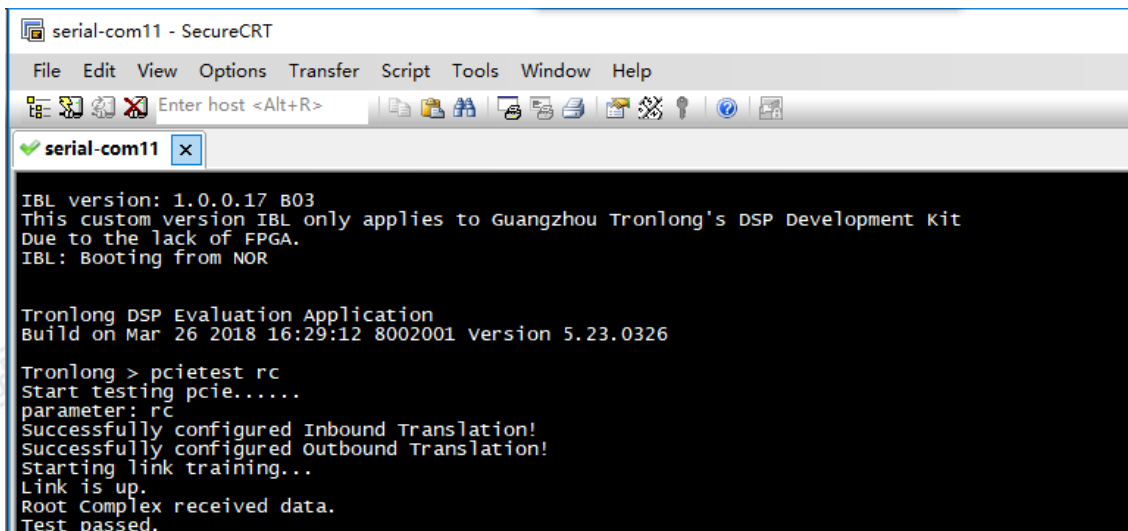
开发板 1 执行以下命令：

Tronlong > pcietest rc

开发板 2 执行以下命令：

Tronlong > pcietest ep

执行完后 PCIe 进行测试，如下图所示：

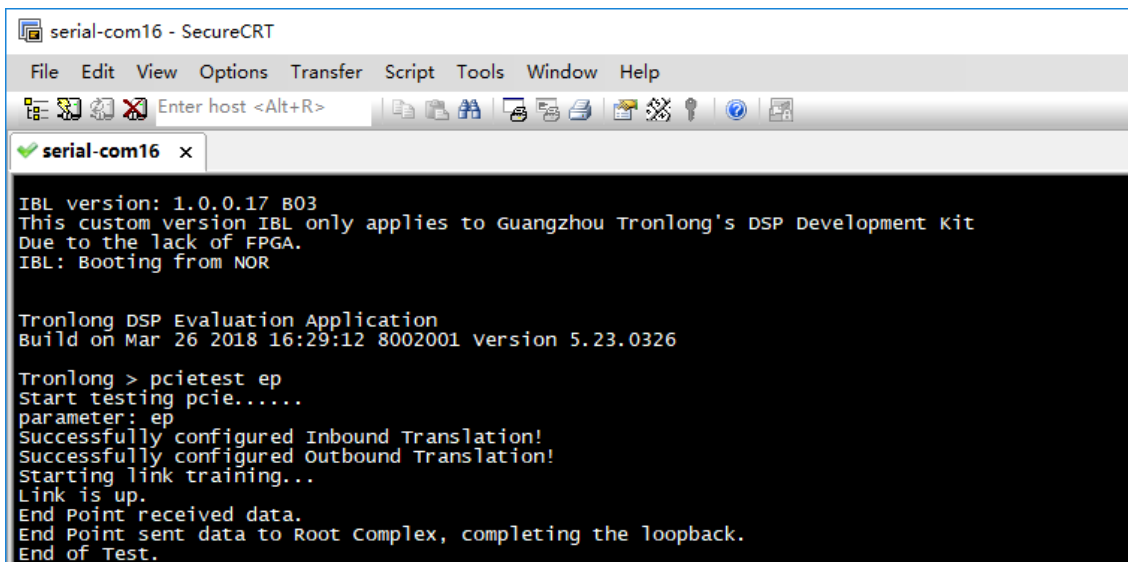


```
serial-com11 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>
serial-com11 x
IBL version: 1.0.0.17 B03
This custom version IBL only applies to Guangzhou Tronlong's DSP Development Kit
Due to the lack of FPGA.
IBL: Booting from NOR

Tronlong DSP Evaluation Application
Build on Mar 26 2018 16:29:12 8002001 Version 5.23.0326

Tronlong > pcietest rc
Start testing pcie.....
parameter: rc
Successfully configured Inbound Translation!
Successfully configured Outbound Translation!
Starting link training...
Link is up.
Root Complex received data.
Test passed.
```

图 22 开发板 1



```
serial-com16 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>
serial-com16 x
IBL version: 1.0.0.17 B03
This custom version IBL only applies to Guangzhou Tronlong's DSP Development Kit
Due to the lack of FPGA.
IBL: Booting from NOR

Tronlong DSP Evaluation Application
Build on Mar 26 2018 16:29:12 8002001 Version 5.23.0326

Tronlong > pcietest ep
Start testing pcie.....
parameter: ep
Successfully configured Inbound Translation!
Successfully configured Outbound Translation!
Starting link training...
Link is up.
End Point received data.
End Point sent data to Root Complex, completing the loopback.
End of Test.
```

图 23 开发板 2

2.1.3 创龙 TMS320C665x DSP 与 FPGA 通信（仅适用于 TL665xF-EasyEVM）

DSP 与 FPGA 通信需要把开发板的拨码开关第 5 位拨到 1，按照 IBL NOR 模式启动开发板。

测试说明：DSP 端通过 TFTP 服务器加载 FPGA 所需的.bit 文件，并在 DSP 端执行命令进行测试。

（1）测试步骤

➤ 部署 TFTP 服务器

打开 TFTP 服务器，路径："光盘资料/Demo/Hostapp/tftpd32.exe"，Current Directory 选择.bit 文件所在路径（非中文），Server interfaces 选择电脑终端的 IP 地址，如下图所示：

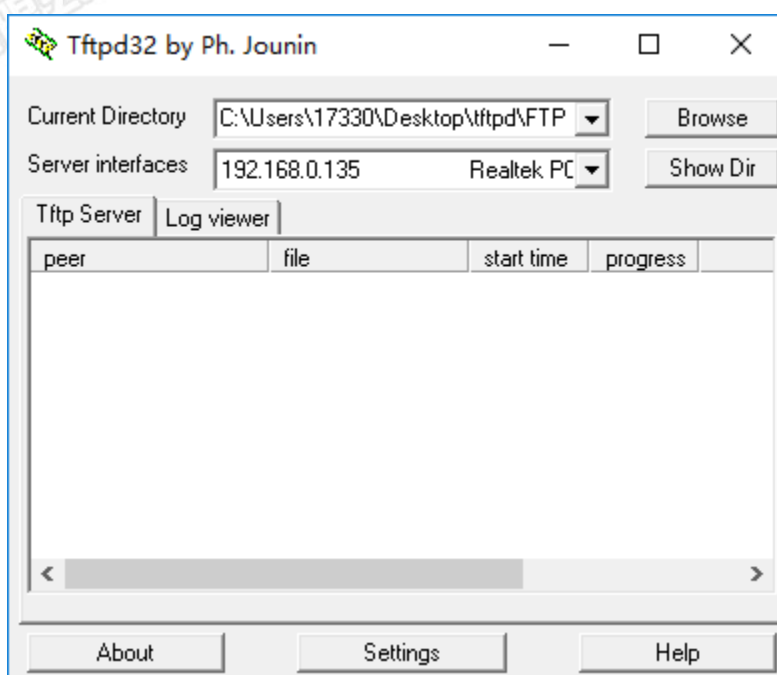


图 24

➤ 启动网络支持

在串口调试终端执行 `ndk dhcp` 命令启动网络支持。


```
Tronlong > ndk dhcp
parameter: dhcp
Service Status:   DHCP:   Enabled:   : 000
Service Status:   Telnet:  Enabled:   : 000
Service Status:   HTTP:   Enabled:   : 000
Service Status:   DHCP:   Enabled:   Running: 000

Network Added: 192.168.1.159
Service Status: DHCP:   Enabled:   Running: 017
DHCP Server ID:
DHCP Server 1 = '192.168.1.1'

Router Information:
Router 1 = '192.168.1.1'
```

图 25

➤ 通过 TFTP 加载 FPGA 镜像

在串口调试终端执行命令加载 FPGA 镜像，命令格式如下：

Tronlong > fpgaprogram tftp [电脑终端 IP] [FPGA 镜像文件名]

以 I2C 镜像为例：

Tronlong > fpgaprogram tftp 192.168.0.135 i2c_test.bit

可以在 tftpd 服务器端看到文件传输进度，文件传输完成后开始编程 FPGA，如下图所示：

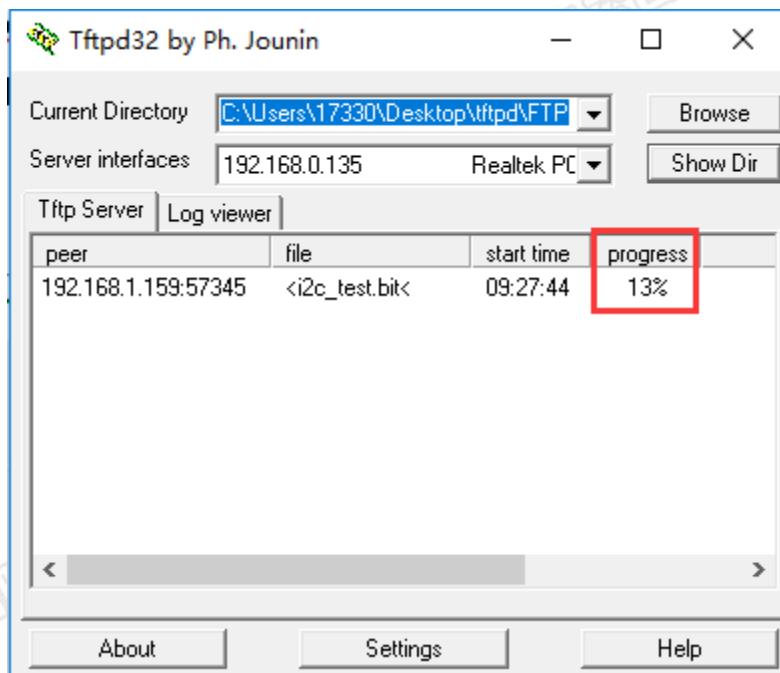


图 26

编程完成后会提示编程结果，如下图所示：

```
Tronlong > fpgaprogram tftp 192.168.0.135 i2c_test.bit  
Tronlong > FPGA has been Programmed successfully!
```

图 27

➤ DSP 端执行测试命令

在串口调试终端执行命令测试 FPGA 镜像，以 I2C 为例，执行以下命令：

Tronlong > fpgai2c

```
Tronlong > fpgai2c
[RO] FPGA ID 0
[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 0
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 0
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 0
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 0
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33
```

图 28

以下测试 DSP 与 FPGA 通过 I2C、EMIF、SRIO 以及文件系统方式通信，FPGA 镜像可在 FPGA 端光盘资料 Demo 中获取。

(2) DSP 与 FPGA I2C 通信测试

按照上述测试步骤加载 I2C 镜像，如下图所示：

```
Tronlong > fpgaprogram tftp 192.168.0.135 i2c_test.bit
Tronlong > FPGA has been Programmed successfully!

Tronlong >
Tronlong > fpgai2c
[RO] FPGA ID 0
[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 1
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 1
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 1
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33

[WO] Light LED
[WO] Quenching LED
[RO] KEY 3 Status 1 KEY 4 Status 1
[RW] Writing FPGA Register #00 11
[RW] Reading FPGA Register #00 11
[RW] Writing FPGA Register #03 22
[RW] Reading FPGA Register #03 22
[RW] Writing FPGA Register #04 33
[RW] Reading FPGA Register #04 33
```

图 29

(3) DSP 与 FPGA SRIO 通信测试

执行以下命令进行 SRIO 通信测试:

Tronlong > fpgaprogram tftp 192.168.0.135 srio_dsp_2x.bit //IP 以实际电脑终端 IP 为准

```
Tronlong > fpgaprogram tftp 192.168.0.135 srio_dsp_2x.bit
Tronlong > FPGA has been Programmed successfully!
```

图 30

Tronlong > fpgasrio

```
Tronlong > fpgasrio
DSP NWRITE FPGA 1024 bytes, 1058 cycles, 7383 Mbps, 922 MB/s, uiCompletionCode 0
DSP NREAD FPGA 1024 bytes, 3145 cycles, 2483 Mbps, 310 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 1024 bytes, 1013 cycles, 7711 Mbps, 963 MB/s, uiCompletionCode 0
DSP NREAD FPGA 1024 bytes, 3141 cycles, 2487 Mbps, 310 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 1024 bytes, 1013 cycles, 7711 Mbps, 963 MB/s, uiCompletionCode 0
DSP NREAD FPGA 1024 bytes, 3141 cycles, 2487 Mbps, 310 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 1024 bytes, 1013 cycles, 7711 Mbps, 963 MB/s, uiCompletionCode 0
DSP NREAD FPGA 1024 bytes, 3141 cycles, 2487 Mbps, 310 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 16384 bytes, 15615 cycles, 8004 Mbps, 1000 MB/s, uiCompletionCode 0
DSP NREAD FPGA 16384 bytes, 21369 cycles, 5849 Mbps, 731 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 16384 bytes, 15615 cycles, 8004 Mbps, 1000 MB/s, uiCompletionCode 0
DSP NREAD FPGA 16384 bytes, 21369 cycles, 5849 Mbps, 731 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 16384 bytes, 15615 cycles, 8004 Mbps, 1000 MB/s, uiCompletionCode 0
DSP NREAD FPGA 16384 bytes, 21369 cycles, 5849 Mbps, 731 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 16384 bytes, 15615 cycles, 8004 Mbps, 1000 MB/s, uiCompletionCode 0
DSP NREAD FPGA 16384 bytes, 21369 cycles, 5849 Mbps, 731 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 32768 bytes, 33375 cycles, 7490 Mbps, 936 MB/s, uiCompletionCode 0
DSP NREAD FPGA 32768 bytes, 40806 cycles, 6126 Mbps, 765 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 32768 bytes, 33391 cycles, 7486 Mbps, 935 MB/s, uiCompletionCode 0
DSP NREAD FPGA 32768 bytes, 40806 cycles, 6126 Mbps, 765 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 32768 bytes, 33391 cycles, 7486 Mbps, 935 MB/s, uiCompletionCode 0
DSP NREAD FPGA 32768 bytes, 40806 cycles, 6126 Mbps, 765 MB/s, uiCompletionCode 0
err = 0
DSP NWRITE FPGA 32768 bytes, 33391 cycles, 7486 Mbps, 935 MB/s, uiCompletionCode 0
DSP NREAD FPGA 32768 bytes, 40806 cycles, 6126 Mbps, 765 MB/s, uiCompletionCode 0
err = 0
```

图 31

(4) DSP 与 FPGA EMIF16 通信测试

执行以下命令进行 EMIF16 通信测试：

Tronlong > fpgaprogram tftp 192.168.0.135 emifa_top.bit

```
Tronlong > fpgaprogram tftp 192.168.0.135 emifa_top.bit
Tronlong > FPGA has been Programmed successfully!
```

图 32

Tronlong > fpgaemif

```
Tronlong > fpgaemif
Starting Writing to FPGA.....Writing 256 words to FPGA
DSP Write to FPGA 512bytes, 181422 cycles, 22.5771961Mbps , 2.8221495MB/s
Reading 256 words to FPGA
DSP Read from FPGA 512bytes, 193446 cycles, 21.1738682Mbps , 2.6467335MB/s
EMIFA transfers complete!
```

图 33

(5) 通过文件系统方式通信

从 DSP 文件系统直接读取 FPGA .bit 文件并加载。

- 可以在串口终端执行 ls 命令查看 DSP FLASH 中存储的 FPGA .bit 文件列表。不同版本程序文件数量可能不同。

Tronlong > ls

```
Tronlong > ls
Working Directory 0:
----A 1997/10/21 12:49      88  HELLO.TXT
----A 1997/10/21 12:49 1152054 LCD.BMP
----A 1997/10/21 12:49 3825888 LED.BIT
----A 1997/10/21 12:49 3825888 KEY.BIT
----A 1997/10/21 12:49 3825893 I2C.BIT
----A 1997/10/21 12:49 3825894 EMIFA.BIT
----A 1997/10/21 12:49 3825894 UART.BIT
----A 1997/10/21 12:49 3825896 SPIO.BIT

 8 File(s), 24107495 bytes total
 0 Dir(s), 9047K bytes free
```

图 34

- 加载 FPGA 镜像

执行以下指令：

Tronlong > fpgaprogram file emifa.bit

```
Tronlong > fpgaprogram file emifa.bit  
FPGA has been Programmed successfully!
```

图 35

由于本地读取速度很快，最快仅需要 6-7 秒即可完成。

- 可以根据测试需要修改 DSP 编程 FPGA 通信时钟
程序默认设置编程时钟为 50MHz，可以根据需要修改编程时钟提高/降低速度。执行以下命令：

Tronlong > fpgaprogram setclock 50000

```
Tronlong > fpgaprogram setclock 50000  
Programming clock SET to 50000000Hz
```

图 36

代表设置编程时钟为 50MHz，最大支持 50MHz。

2.2 创龙 TMS320C665x NAND FLASH 启动测试

将开发板的拨码开关拨到 IBL NAND 模式，这个档位是 IBL NAND FLASH 启动模式，是二级启动程序。开发板上电后，串口终端会打印信息如下图：

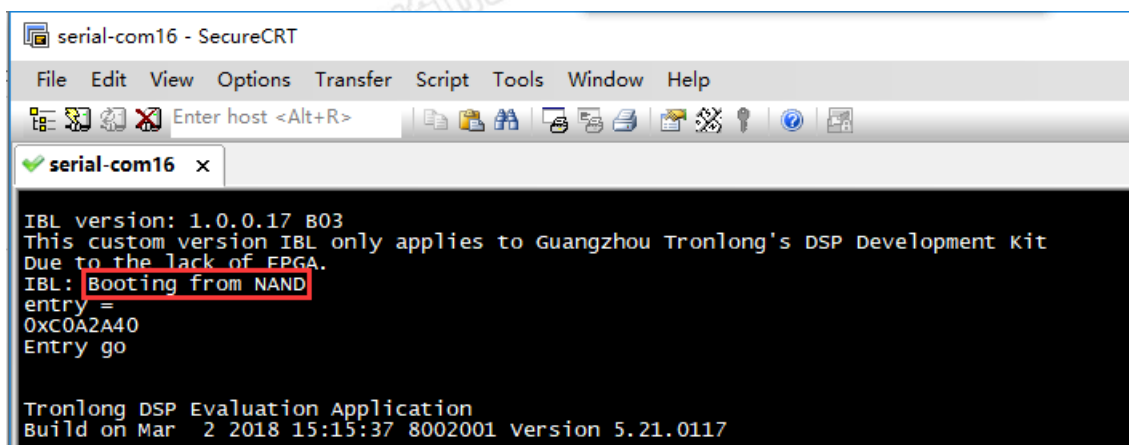


图 37

创龙 TMS320C665x 更多帮助

销售邮箱: sales@tronlong.com

技术邮箱: support@tronlong.com

创龙总机: 020-8998-6280

技术热线: 020-3893-9734

创龙官网: www.tronlong.com

技术论坛: www.51ele.net

线上商城: <https://tronlong.taobao.com>