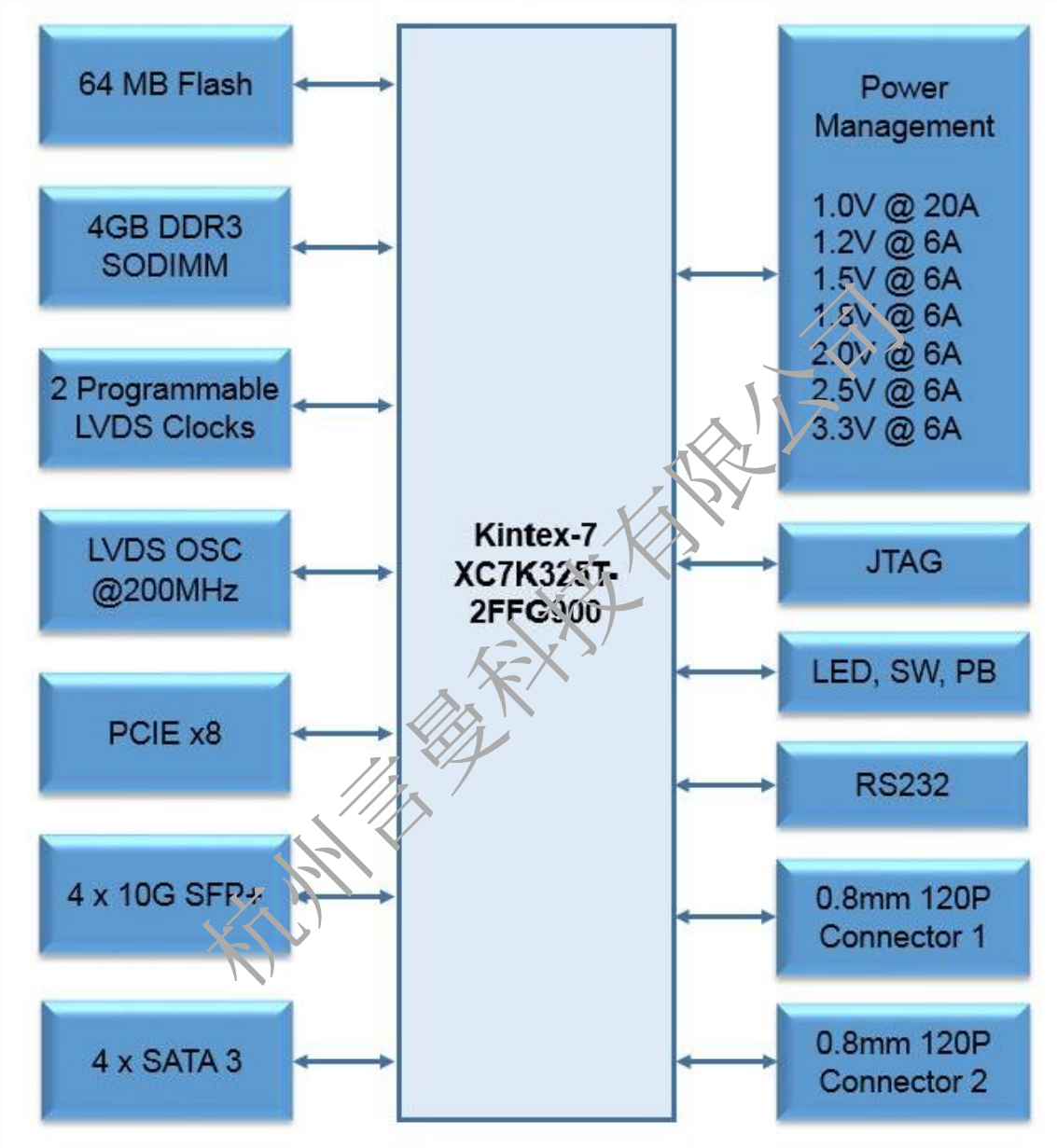
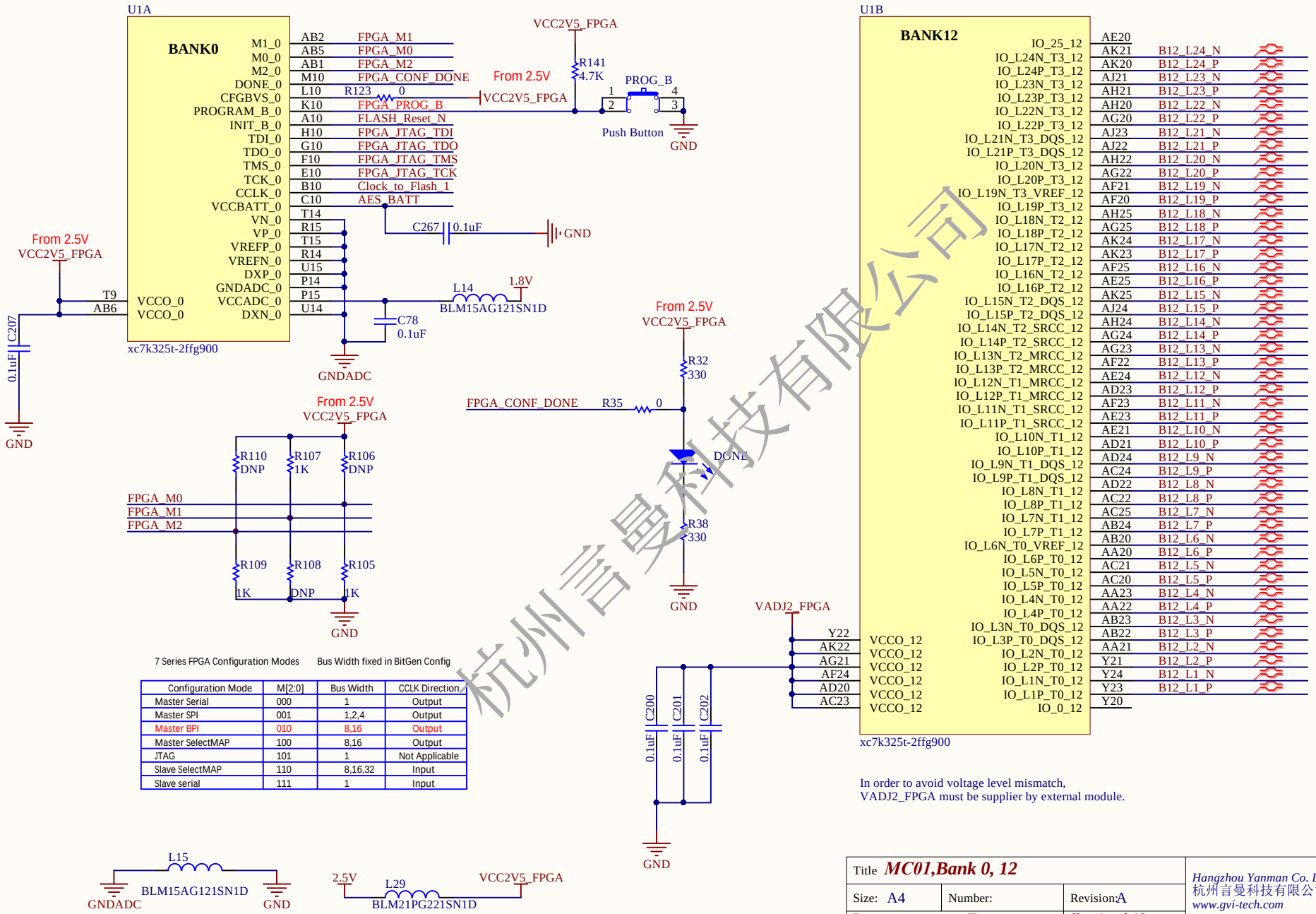
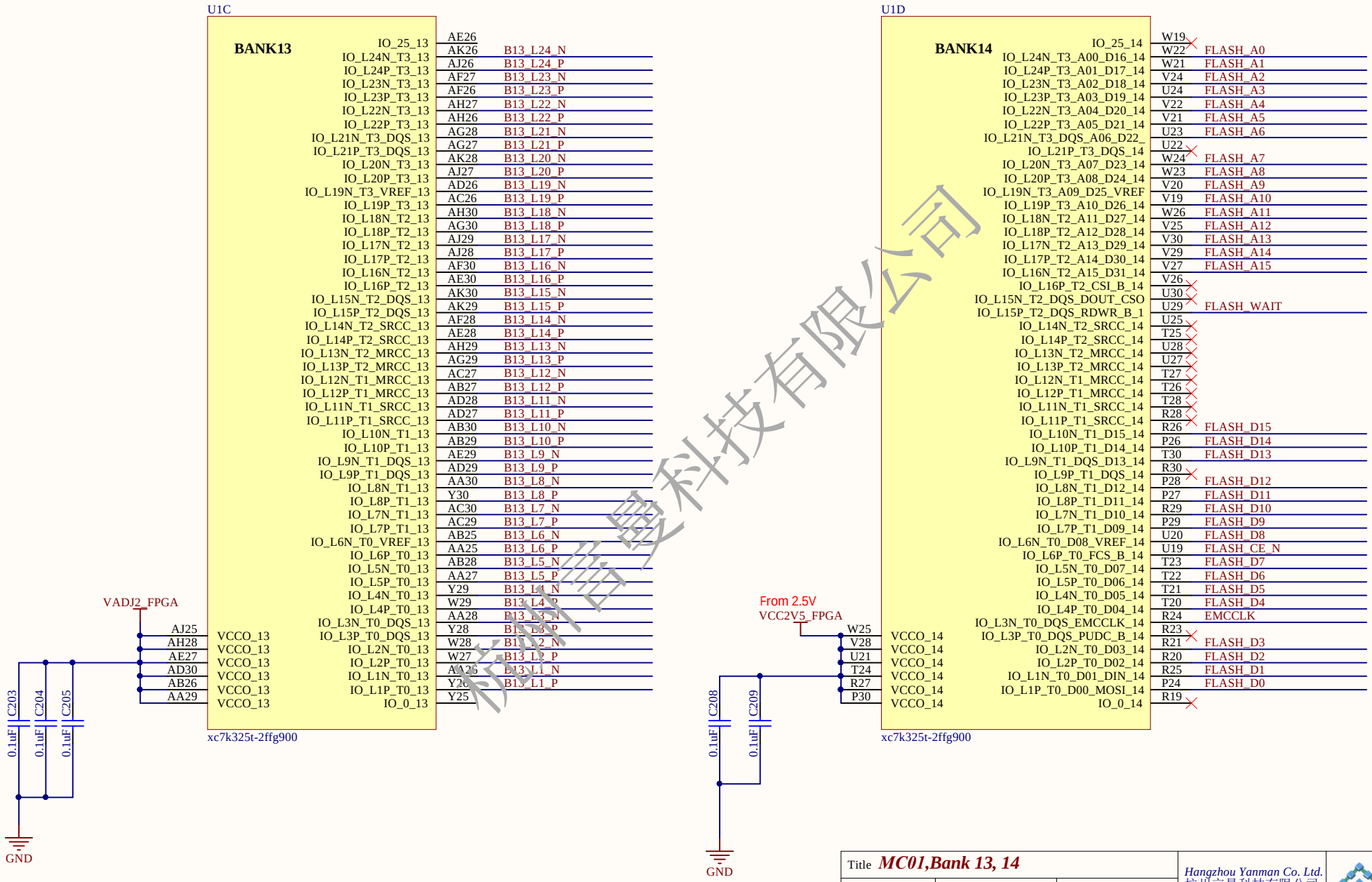
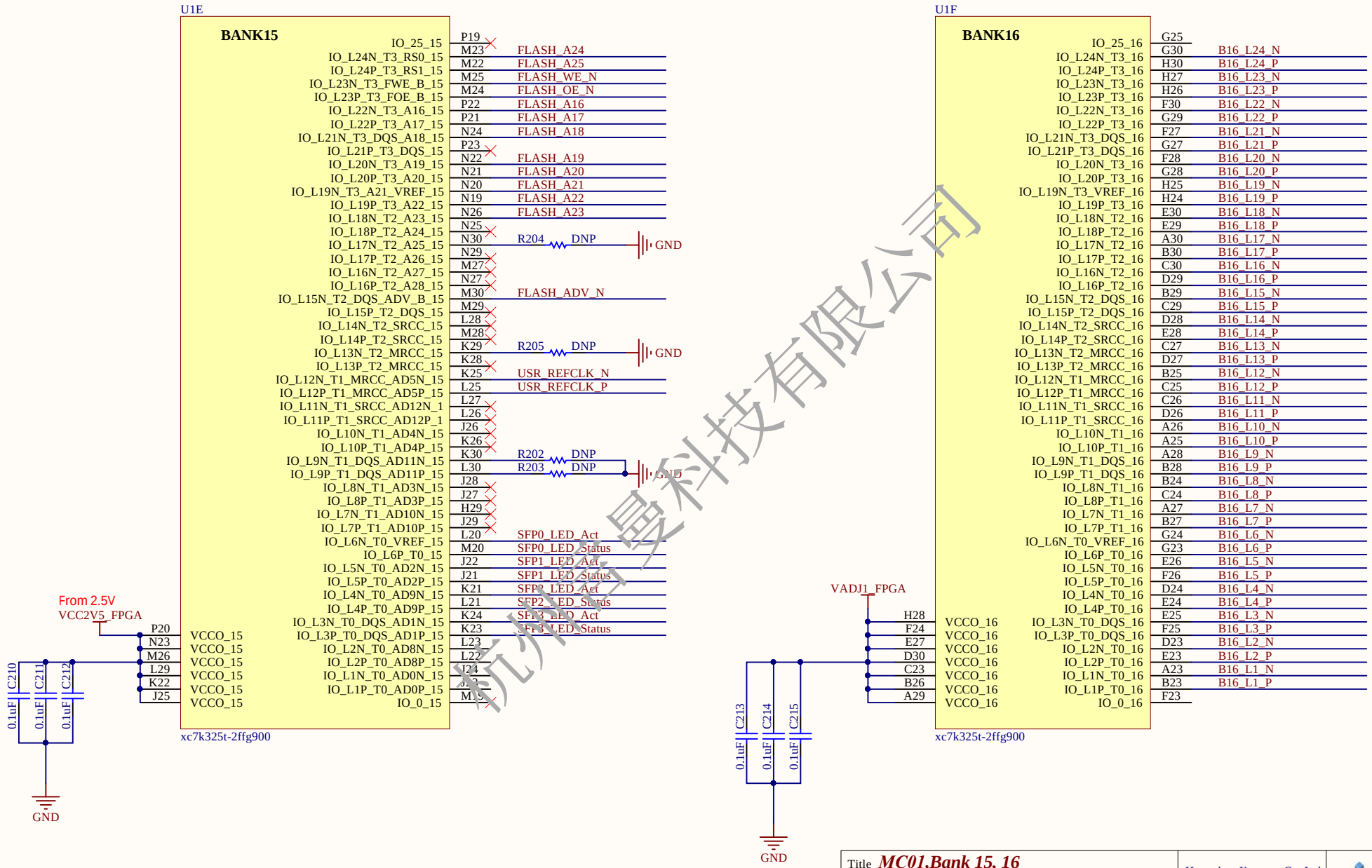


Title *MC01,Block Diagram*			*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet1 of 23	
File:			

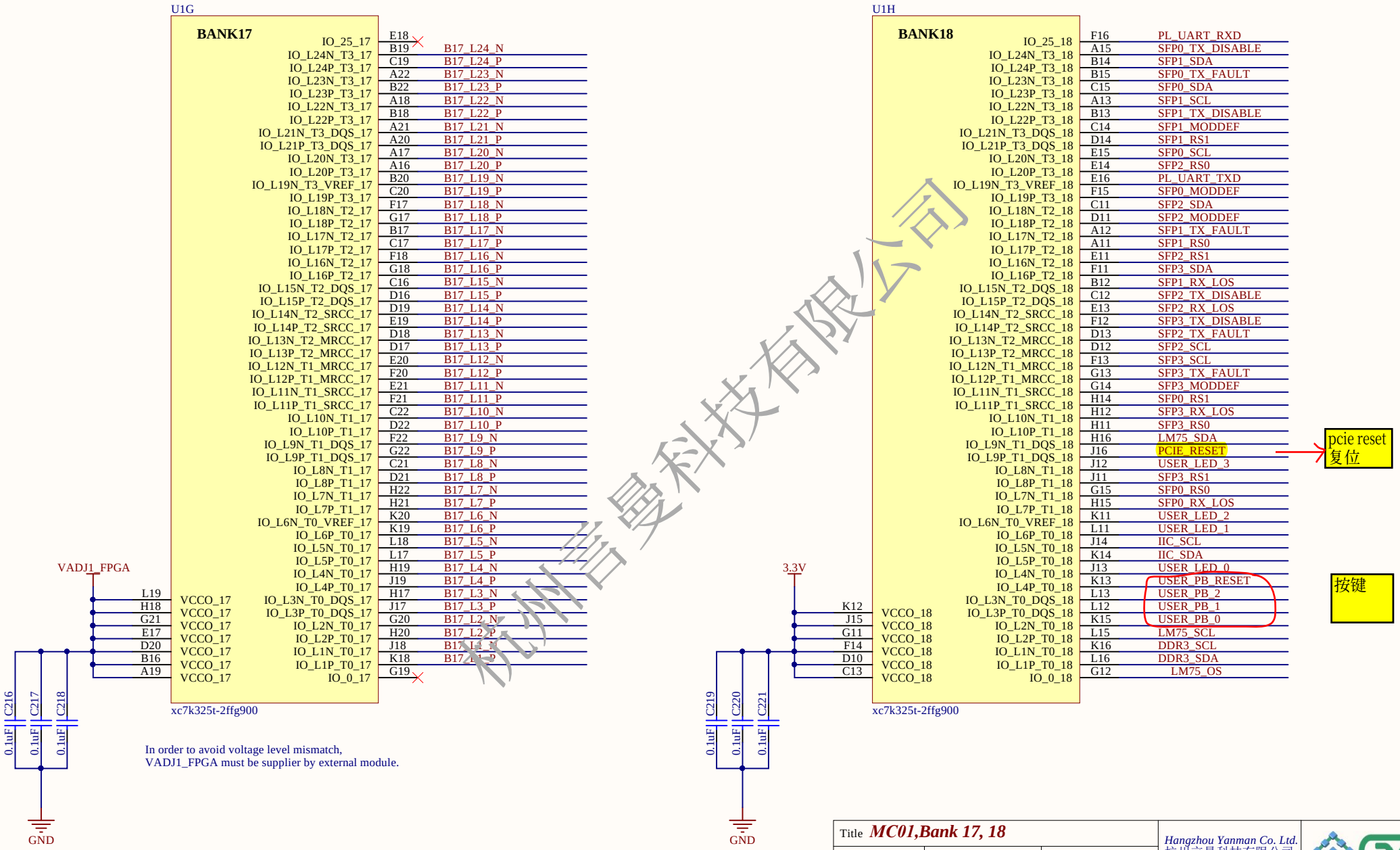

U1A
BANK0
xc7k325t-2ffg900
M1_0 AB2 FPGA_M1
M0_0 AB5 FPGA_M0
M2_0 AB1 FPGA_M2
DONE_0 M10 FPGA_CONF_DONE
CFGBVS_0 L10
PROGRAM_B_0 K10 FPGA_PROG_B
INIT_B_0 A10 FLASH_Reset_N
TDI_0 H10 FPGA_JTAG_TDI
TDO_0 G10 FPGA_JTAG_TDO
TMS_0 F10 FPGA_JTAG_TMS
TCK_0 E10 FPGA_JTAG_TCK
CCLK_0 B10 Clock_to_Flash_1
VCCBATT_0 C10 AES_BATT
VN_0 T14
VP_0 R15
VREFP_0 T15
VREFN_0 R14
DXP_0 U15
GNDADC_0 P14
VCCADC_0 P15
DXN_0 U14
VCCO_0 T9
VCCO_0 AB6
R123 0
From 2.5V
VCC2V5_FPGA
R141 4.7K
PROG_B
Push Button
GND
C267 0.1uF
L14 1.8V
BLM15AG121SN1D
C78 0.1uF
GNDADC
C207 0.1uF
R110 DNP
R107 1K
R106 DNP
R109 1K
R108 DNP
R105 1K
FPGA_M0
FPGA_M1
FPGA_M2
FPGA_CONF_DONE
R35 0
R32 330
R38 330
DONE
U1B
BANK12
IO_25_12 AE20
IO_L24N_T3_12 AK21 B12_L24_N
IO_L24P_T3_12 AK20 B12_L24_P
IO_L23N_T3_12 AJ21 B12_L23_N
IO_L23P_T3_12 AH21 B12_L23_P
IO_L22N_T3_12 AH20 B12_L22_N
IO_L22P_T3_12 AG20 B12_L22_P
IO_L21N_T3_DQS_12 AJ23 B12_L21_N
IO_L21P_T3_DQS_12 AJ22 B12_L21_P
IO_L20N_T3_12 AH22 B12_L20_N
IO_L20P_T3_12 AG22 B12_L20_P
IO_L19N_T3_VREF_12 AF21 B12_L19_N
IO_L19P_T3_12 AF20 B12_L19_P
IO_L18N_T2_12 AH25 B12_L18_N
IO_L18P_T2_12 AG25 B12_L18_P
IO_L17N_T2_12 AK24 B12_L17_N
IO_L17P_T2_12 AK23 B12_L17_P
IO_L16N_T2_12 AF25 B12_L16_N
IO_L16P_T2_12 AE25 B12_L16_P
IO_L15N_T2_DQS_12 AK25 B12_L15_N
IO_L15P_T2_DQS_12 AJ24 B12_L15_P
IO_L14N_T2_SRCC_12 AH24 B12_L14_N
IO_L14P_T2_SRCC_12 AG24 B12_L14_P
IO_L13N_T2_MRCC_12 AG23 B12_L13_N
IO_L13P_T2_MRCC_12 AF22 B12_L13_P
IO_L12N_T1_MRCC_12 AE24 B12_L12_N
IO_L12P_T1_MRCC_12 AD23 B12_L12_P
IO_L11N_T1_SRCC_12 AF23 B12_L11_N
IO_L11P_T1_SRCC_12 AE23 B12_L11_P
IO_L10N_T1_12 AE21 B12_L10_N
IO_L10P_T1_12 AD21 B12_L10_P
IO_L9N_T1_DQS_12 AD24 B12_L9_N
IO_L9P_T1_DQS_12 AC24 B12_L9_P
IO_L8N_T1_12 AD22 B12_L8_N
IO_L8P_T1_12 AC22 B12_L8_P
IO_L7N_T1_12 AC25 B12_L7_N
IO_L7P_T1_12 AB24 B12_L7_P
IO_L6N_T0_VREF_12 AB20 B12_L6_N
IO_L6P_T0_12 AA20 B12_L6_P
IO_L5N_T0_12 AC21 B12_L5_N
IO_L5P_T0_12 AC20 B12_L5_P
IO_L4N_T0_12 AA23 B12_L4_N
IO_L4P_T0_12 AA22 B12_L4_P
IO_L3N_T0_DQS_12 AB23 B12_L3_N
IO_L3P_T0_DQS_12 AB22 B12_L3_P
IO_L2N_T0_12 AA21 B12_L2_N
IO_L2P_T0_12 Y21 B12_L2_P
IO_L1N_T0_12 Y24 B12_L1_N
IO_L1P_T0_12 Y23 B12_L1_P
IO_0_12 Y20
VCCO_12 Y22
VCCO_12 AK22
VCCO_12 AG21
VCCO_12 AF24
VCCO_12 AD20
VCCO_12 AC23
xc7k325t-2ffg900
VADJ2_FPGA
C200 0.1uF
C201 0.1uF
C202 0.1uF
In order to avoid voltage level mismatch,
VADJ2_FPGA must be supplier by external module.
7 Series FPGA Configuration Modes
Bus Width fixed in BitGen Config
Configuration Mode | M[2:0] | Bus Width | CCLK Direction
Master Serial | 000 | 1 | Output
Master SPI | 001 | 1,2,4 | Output
Master BPI | 010 | 8,16 | Output
Master SelectMAP | 100 | 8,16 | Output
JTAG | 101 | 1 | Not Applicable
Slave SelectMAP | 110 | 8,16,32 | Input
Slave serial | 111 | 1 | Input
L15
BLM15AG121SN1D
GNDADC
GND
2.5V
L29
BLM21PG221SN1D
VCC2V5_FPGA
Title MC01,Bank 0, 12
Size: A4
Number:
Revision:A
Date:
Time:
Sheet2 of 23
File:
Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com


U1C
BANK13
IO_25_13 AE26
IO_L24N_T3_13 AK26 B13_L24_N
IO_L24P_T3_13 AJ26 B13_L24_P
IO_L23N_T3_13 AF27 B13_L23_N
IO_L23P_T3_13 AF26 B13_L23_P
IO_L22N_T3_13 AH27 B13_L22_N
IO_L22P_T3_13 AH26 B13_L22_P
IO_L21N_T3_DQS_13 AG28 B13_L21_N
IO_L21P_T3_DQS_13 AG27 B13_L21_P
IO_L20N_T3_13 AK28 B13_L20_N
IO_L20P_T3_13 AJ27 B13_L20_P
IO_L19N_T3_VREF_13 AD26 B13_L19_N
IO_L19P_T3_13 AC26 B13_L19_P
IO_L18N_T2_13 AH30 B13_L18_N
IO_L18P_T2_13 AG30 B13_L18_P
IO_L17N_T2_13 AJ29 B13_L17_N
IO_L17P_T2_13 AJ28 B13_L17_P
IO_L16N_T2_13 AF30 B13_L16_N
IO_L16P_T2_13 AE30 B13_L16_P
IO_L15N_T2_DQS_13 AK30 B13_L15_N
IO_L15P_T2_DQS_13 AK29 B13_L15_P
IO_L14N_T2_SRCC_13 AF28 B13_L14_N
IO_L14P_T2_SRCC_13 AE28 B13_L14_P
IO_L13N_T2_MRCC_13 AH29 B13_L13_N
IO_L13P_T2_MRCC_13 AG29 B13_L13_P
IO_L12N_T1_MRCC_13 AC27 B13_L12_N
IO_L12P_T1_MRCC_13 AB27 B13_L12_P
IO_L11N_T1_SRCC_13 AD28 B13_L11_N
IO_L11P_T1_SRCC_13 AD27 B13_L11_P
IO_L10N_T1_13 AB30 B13_L10_N
IO_L10P_T1_13 AB29 B13_L10_P
IO_L9N_T1_DQS_13 AE29 B13_L9_N
IO_L9P_T1_DQS_13 AD29 B13_L9_P
IO_L8N_T1_13 AA30 B13_L8_N
IO_L8P_T1_13 Y30 B13_L8_P
IO_L7N_T1_13 AC30 B13_L7_N
IO_L7P_T1_13 AC29 B13_L7_P
IO_L6N_T0_VREF_13 AB25 B13_L6_N
IO_L6P_T0_13 AA25 B13_L6_P
IO_L5N_T0_13 AB28 B13_L5_N
IO_L5P_T0_13 AA27 B13_L5_P
IO_L4N_T0_13 Y29 B13_L4_N
IO_L4P_T0_13 W29 B13_L4_P
IO_L3N_T0_DQS_13 AA28 B13_L3_N
IO_L3P_T0_DQS_13 Y28 B13_L3_P
IO_L2N_T0_13 W28 B13_L2_N
IO_L2P_T0_13 W27 B13_L2_P
IO_L1N_T0_13 AA26 B13_L1_N
IO_L1P_T0_13 Y26 B13_L1_P
IO_0_13 Y25
VCCO_13 AJ25
VCCO_13 AH28
VCCO_13 AE27
VCCO_13 AD30
VCCO_13 AB26
VCCO_13 AA29
xc7k325t-2ffg900
VADJ2_FPGA
C203 0.1uF
C204 0.1uF
C205 0.1uF
GND
U1D
BANK14
IO_25_14 W19
IO_L24N_T3_A00_D16_14 W22 FLASH_A0
IO_L24P_T3_A01_D17_14 W21 FLASH_A1
IO_L23N_T3_A02_D18_14 V24 FLASH_A2
IO_L23P_T3_A03_D19_14 U24 FLASH_A3
IO_L22N_T3_A04_D20_14 V22 FLASH_A4
IO_L22P_T3_A05_D21_14 V21 FLASH_A5
IO_L21N_T3_DQS_A06_D22_ U23 FLASH_A6
IO_L21P_T3_DQS_14 U22
IO_L20N_T3_A07_D23_14 W24 FLASH_A7
IO_L20P_T3_A08_D24_14 W23 FLASH_A8
IO_L19N_T3_A09_D25_VREF V20 FLASH_A9
IO_L19P_T3_A10_D26_14 V19 FLASH_A10
IO_L18N_T2_A11_D27_14 W26 FLASH_A11
IO_L18P_T2_A12_D28_14 V25 FLASH_A12
IO_L17N_T2_A13_D29_14 V30 FLASH_A13
IO_L17P_T2_A14_D30_14 V29 FLASH_A14
IO_L16N_T2_A15_D31_14 V27 FLASH_A15
IO_L16P_T2_CSI_B_14 V26
IO_L15N_T2_DQS_DOUT_CSO U30
IO_L15P_T2_DQS_RDWR_B_1 U29 FLASH_WAIT
IO_L14N_T2_SRCC_14 U25
IO_L14P_T2_SRCC_14 T25
IO_L13N_T2_MRCC_14 U28
IO_L13P_T2_MRCC_14 U27
IO_L12N_T1_MRCC_14 T27
IO_L12P_T1_MRCC_14 T26
IO_L11N_T1_SRCC_14 T28
IO_L11P_T1_SRCC_14 R28
IO_L10N_T1_D15_14 R26 FLASH_D15
IO_L10P_T1_D14_14 P26 FLASH_D14
IO_L9N_T1_DQS_D13_14 T30 FLASH_D13
IO_L9P_T1_DQS_14 R30
IO_L8N_T1_D12_14 P28 FLASH_D12
IO_L8P_T1_D11_14 P27 FLASH_D11
IO_L7N_T1_D10_14 R29 FLASH_D10
IO_L7P_T1_D09_14 P29 FLASH_D9
IO_L6N_T0_D08_VREF_14 U20 FLASH_D8
IO_L6P_T0_FCS_B_14 U19 FLASH_CE_N
IO_L5N_T0_D07_14 T23 FLASH_D7
IO_L5P_T0_D06_14 T22 FLASH_D6
IO_L4N_T0_D05_14 T21 FLASH_D5
IO_L4P_T0_D04_14 T20 FLASH_D4
IO_L3N_T0_DQS_EMCCLK_14 R24 EMCCLK
IO_L3P_T0_DQS_PUDC_B_14 R23
IO_L2N_T0_D03_14 R21 FLASH_D3
IO_L2P_T0_D02_14 R20 FLASH_D2
IO_L1N_T0_D01_DIN_14 R25 FLASH_D1
IO_L1P_T0_D00_MOSI_14 P24 FLASH_D0
IO_0_14 R19
VCCO_14 W25
VCCO_14 V28
VCCO_14 U21
VCCO_14 T24
VCCO_14 R27
VCCO_14 P30
VCCO_14
xc7k325t-2ffg900
From 2.5V
VCC2V5_FPGA
C208 0.1uF
C209 0.1uF
GND
Title MC01,Bank 13, 14
Size: A4
Number:
Revision:A
Date:
Time:
Sheet3 of 23
File:
Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com



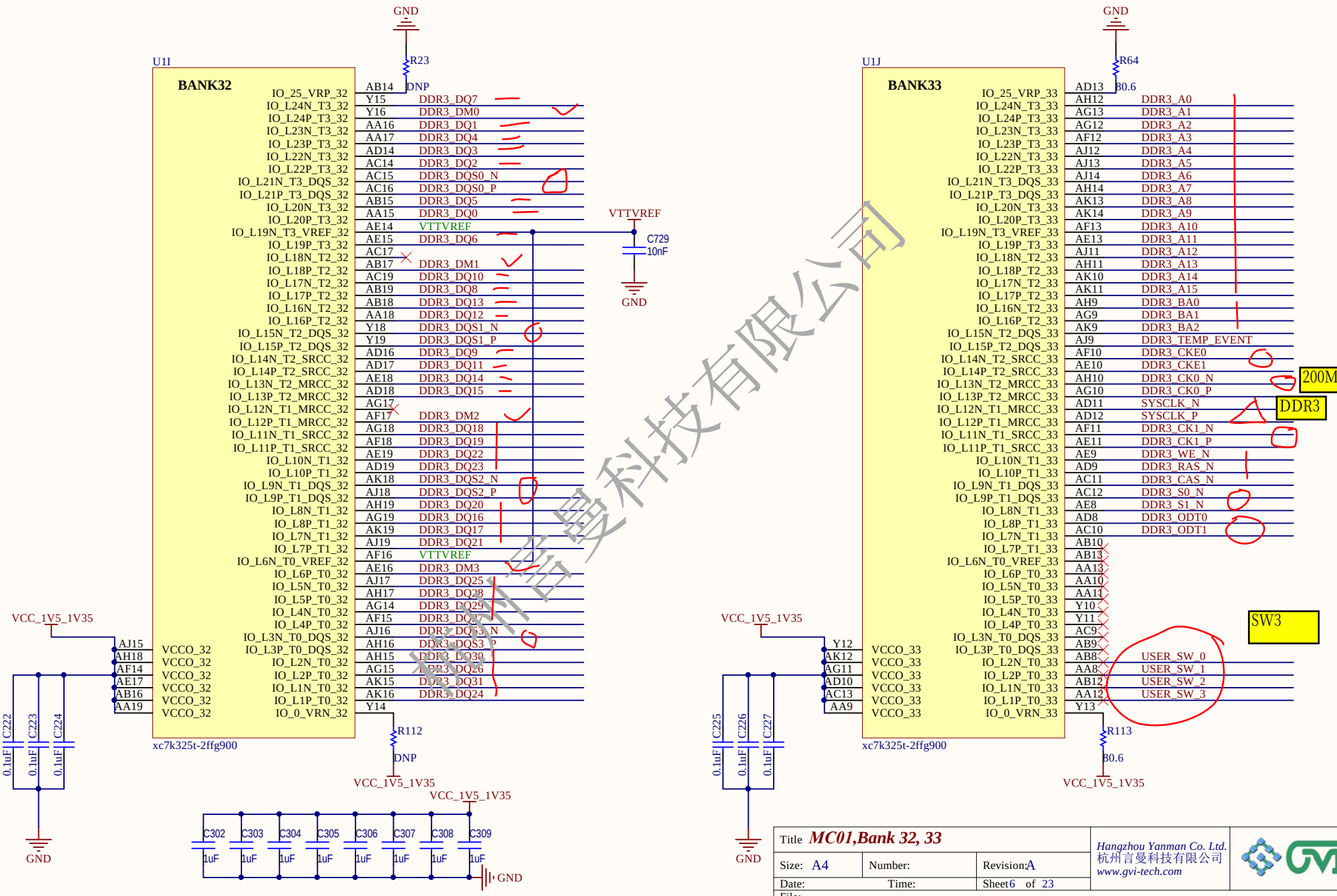
Title	*MC01,Bank 15, 16*		
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet 4 of 23	
File:			

Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com



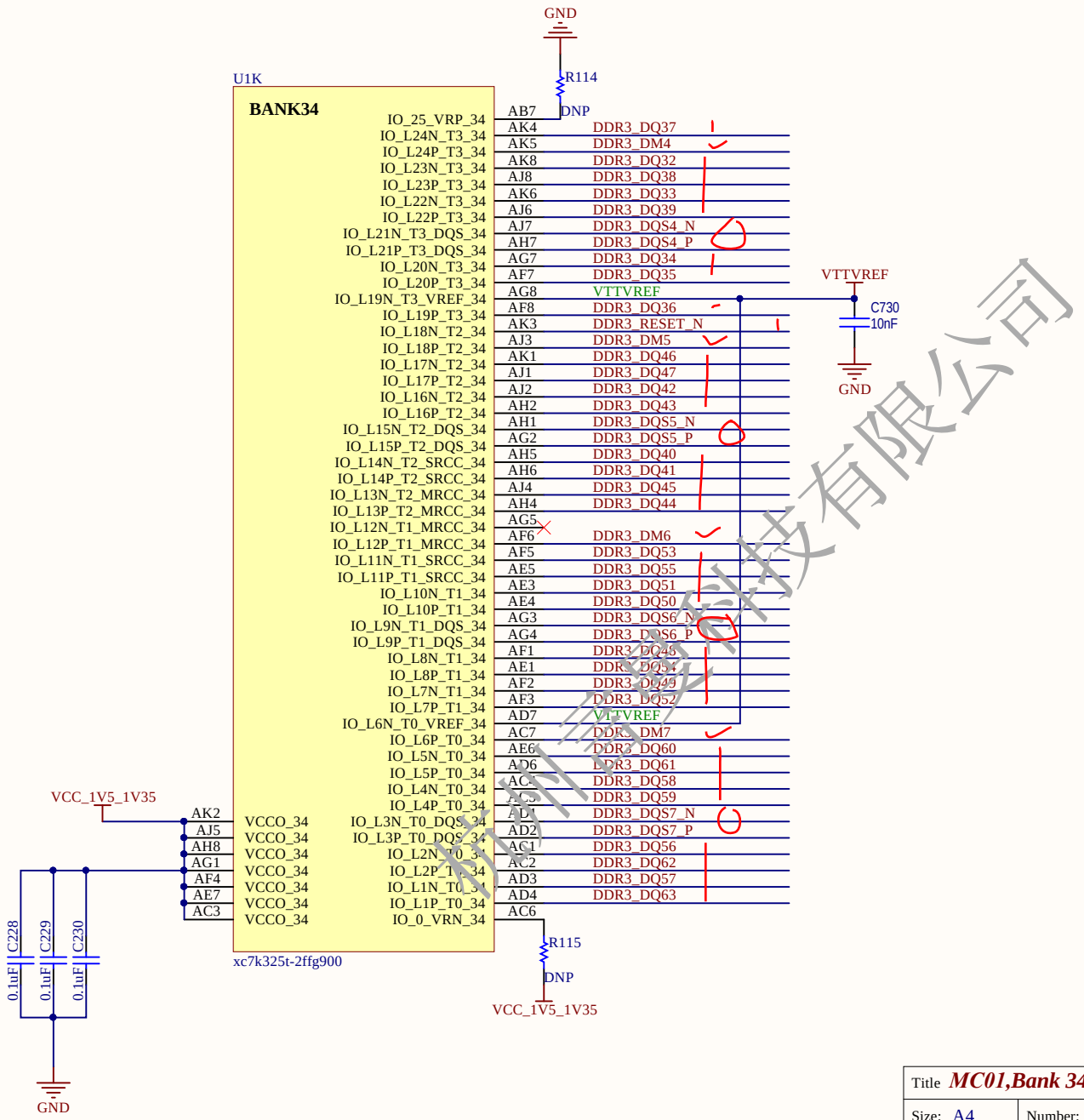
Title: *MC01,Bank 17, 18*		
Size: A4	Number:	Revision: A
Date:	Time:	Sheet 5 of 23
File:		

Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com

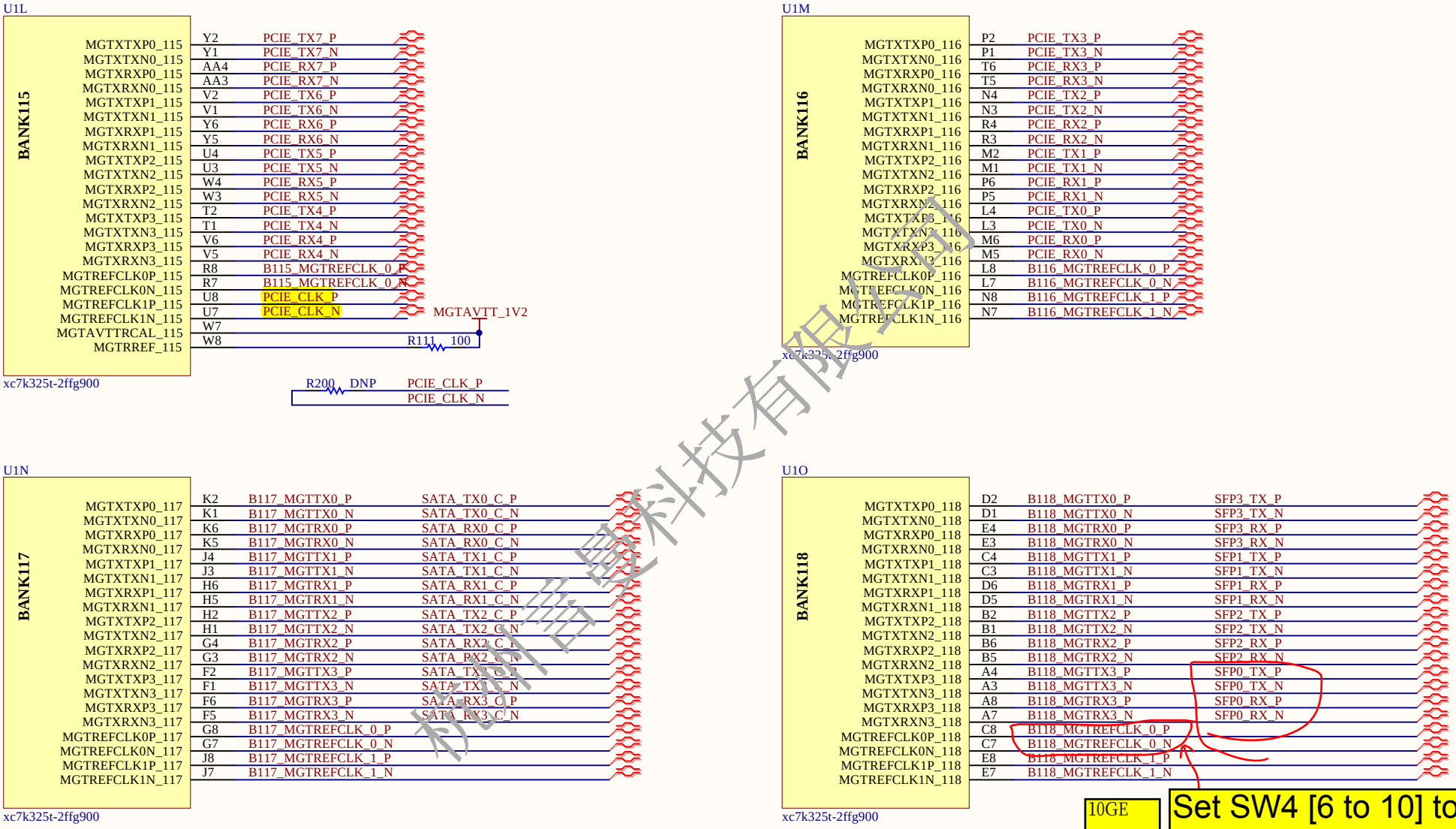


Title: *MC01,Bank 32, 33*		
Size: A4	Number:	Revision:A
Date:	Time:	Sheet 6 of 23
File:		

Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com

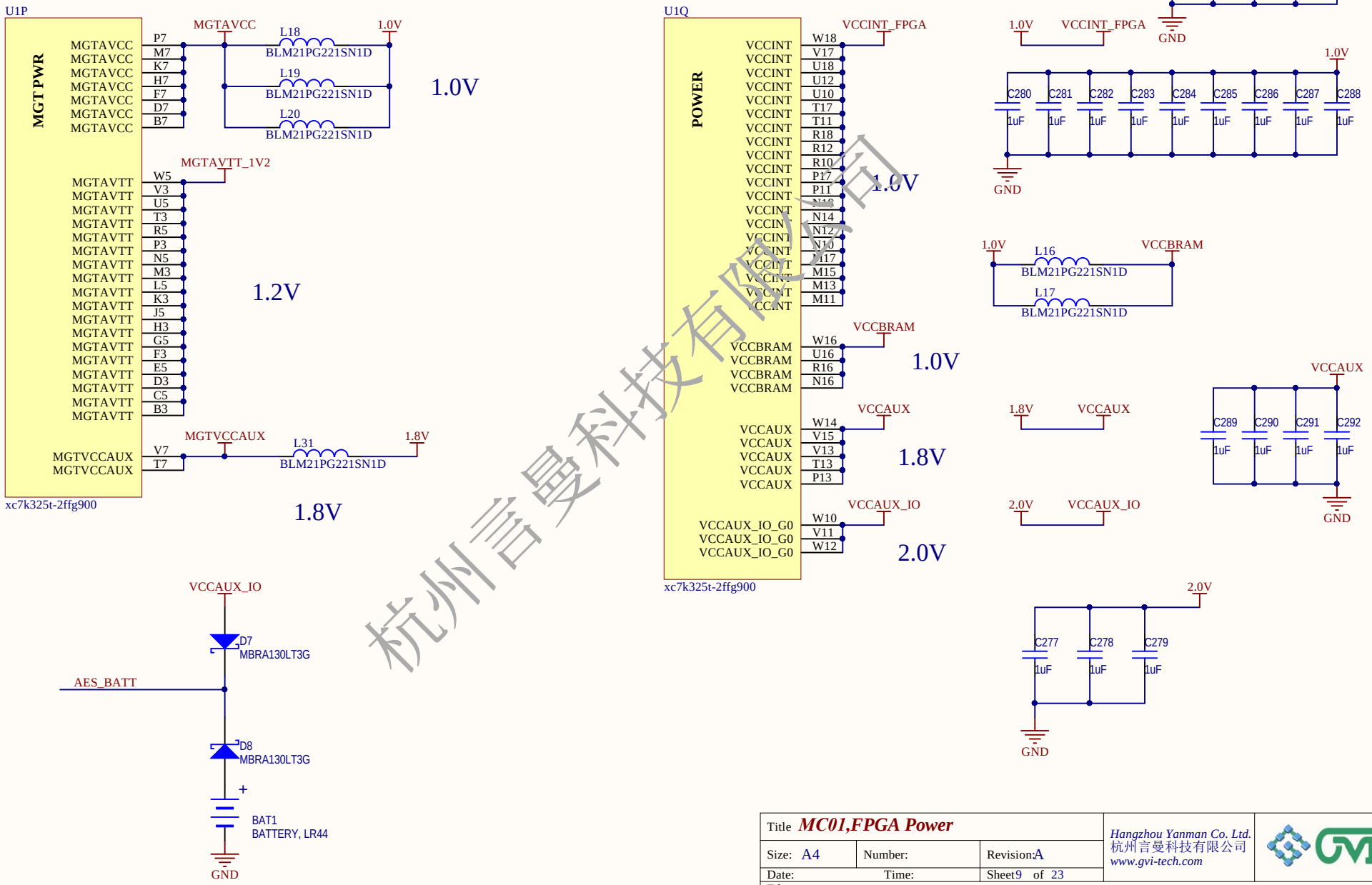


Title	*MC01,Bank 34*		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet7 of 23	
File:			



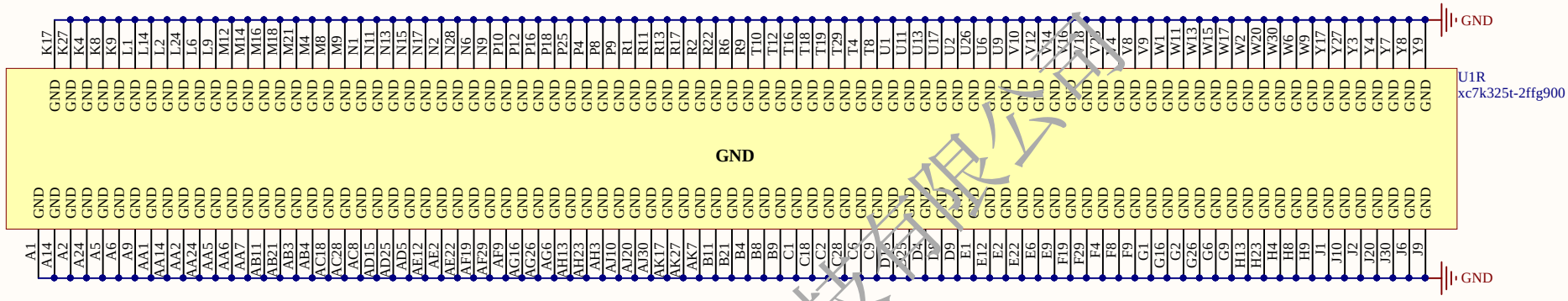
Title: *MC01,Bank GT*		
Size: A4	Number:	Revision: A
Date:	Time:	Sheet 8 of 23
File:		

Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com

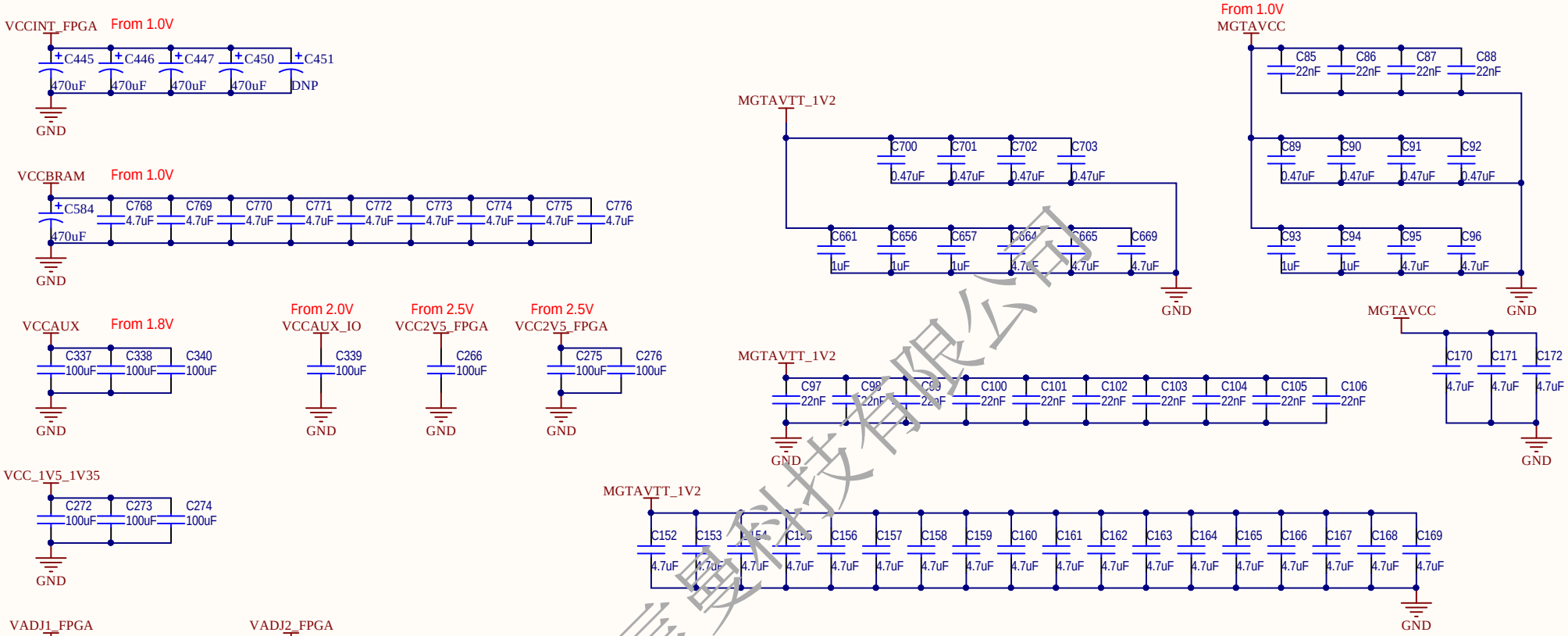


Title	***MC01,FPGA Power***		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet9 of 23	
File:			

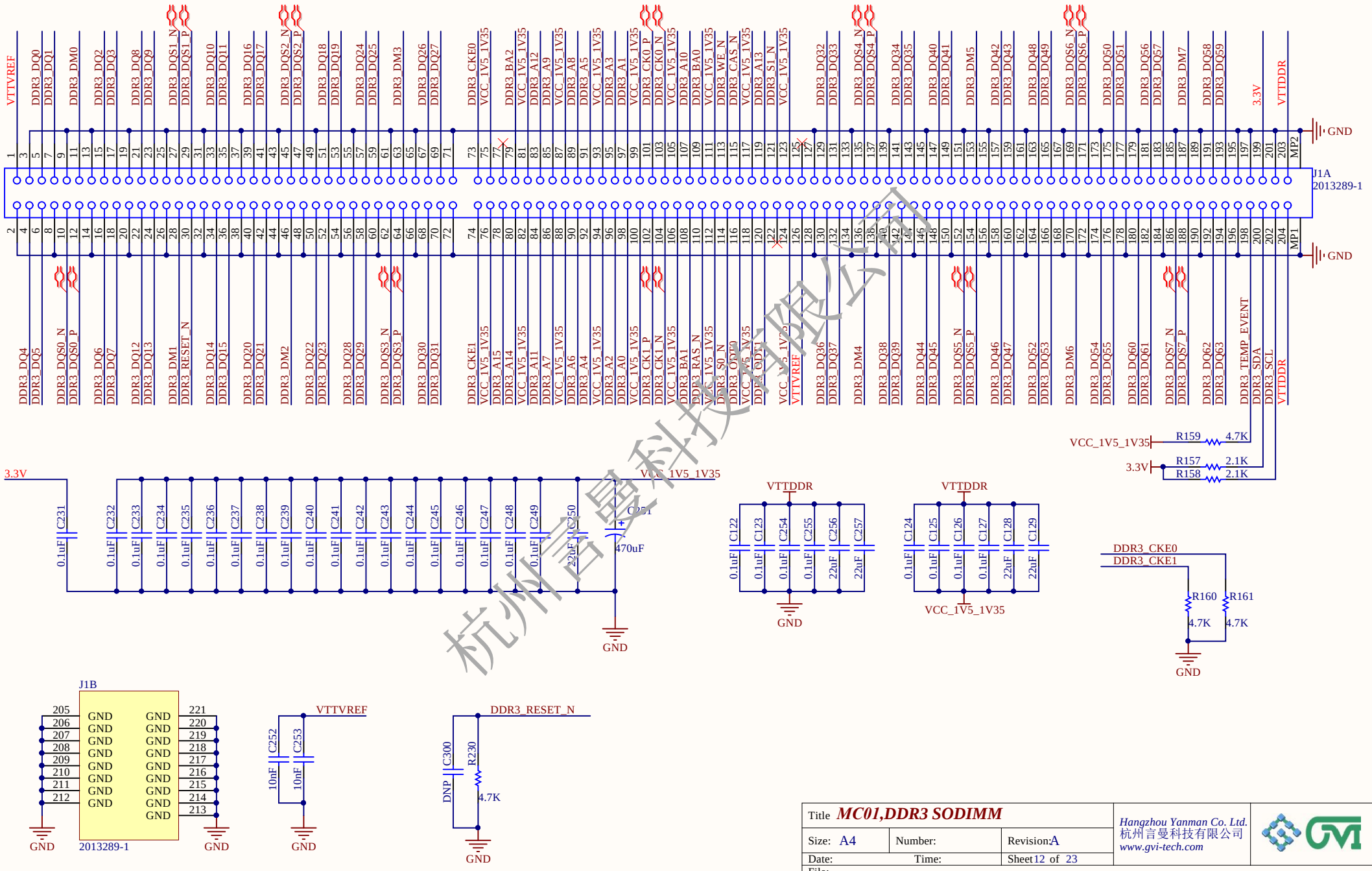
MH1 MH2



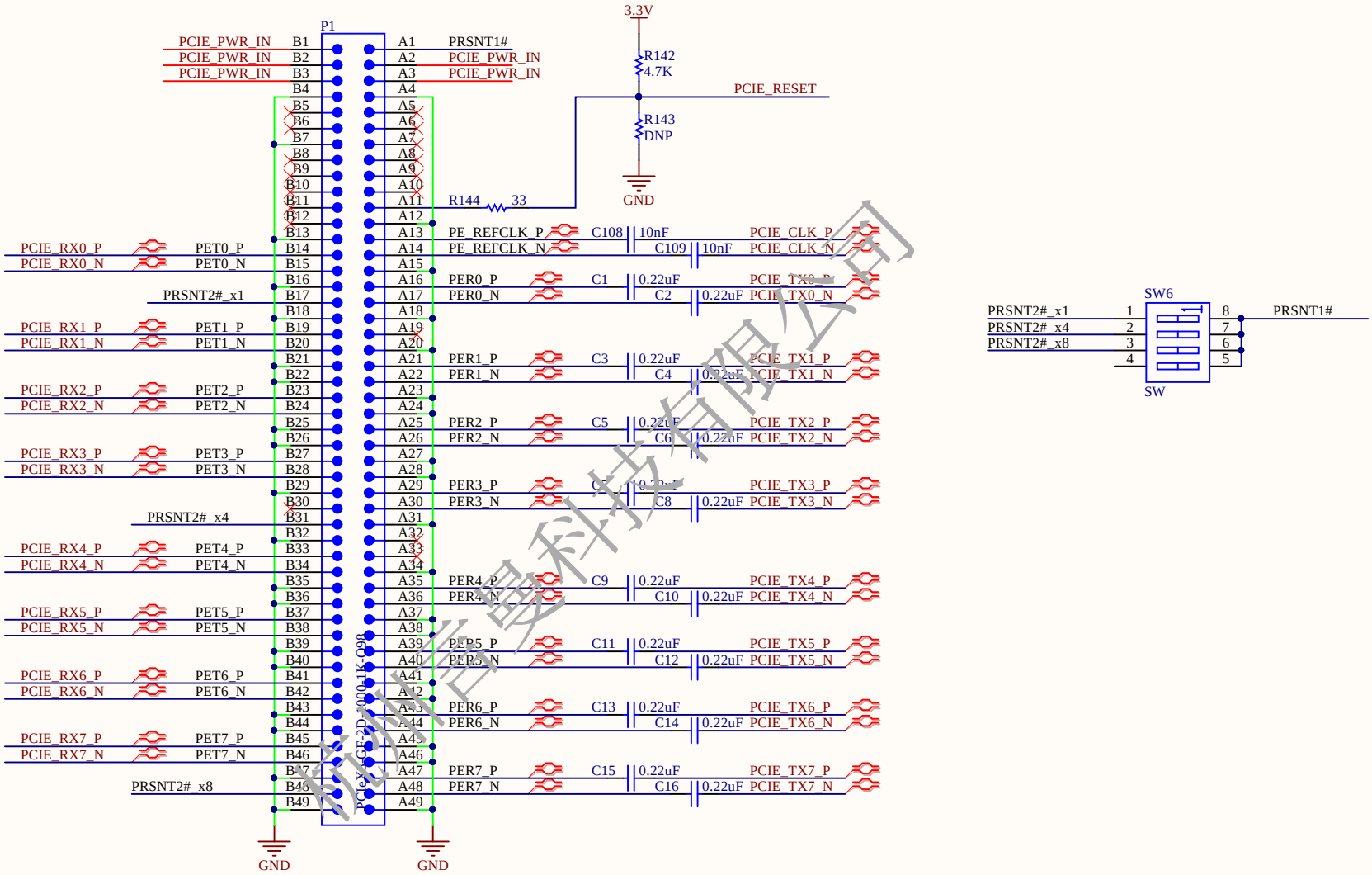
Title: *MC01,FPGA GND*			*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision: A	
Date:	Time:	Sheet 10 of 23	
File:			



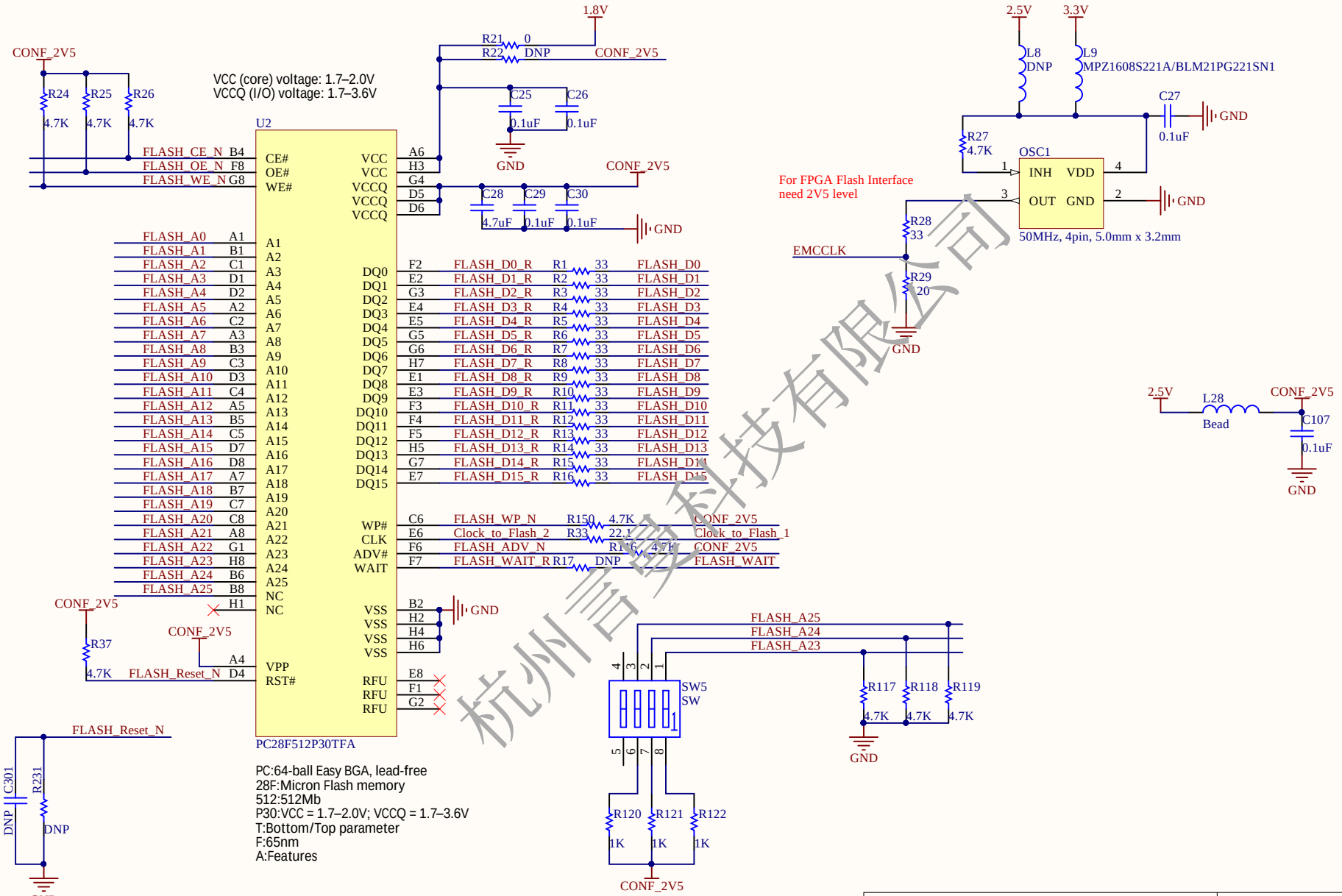
Title	***MC01, PWR Bypass Capacitors***		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet11 of 23	
File:			



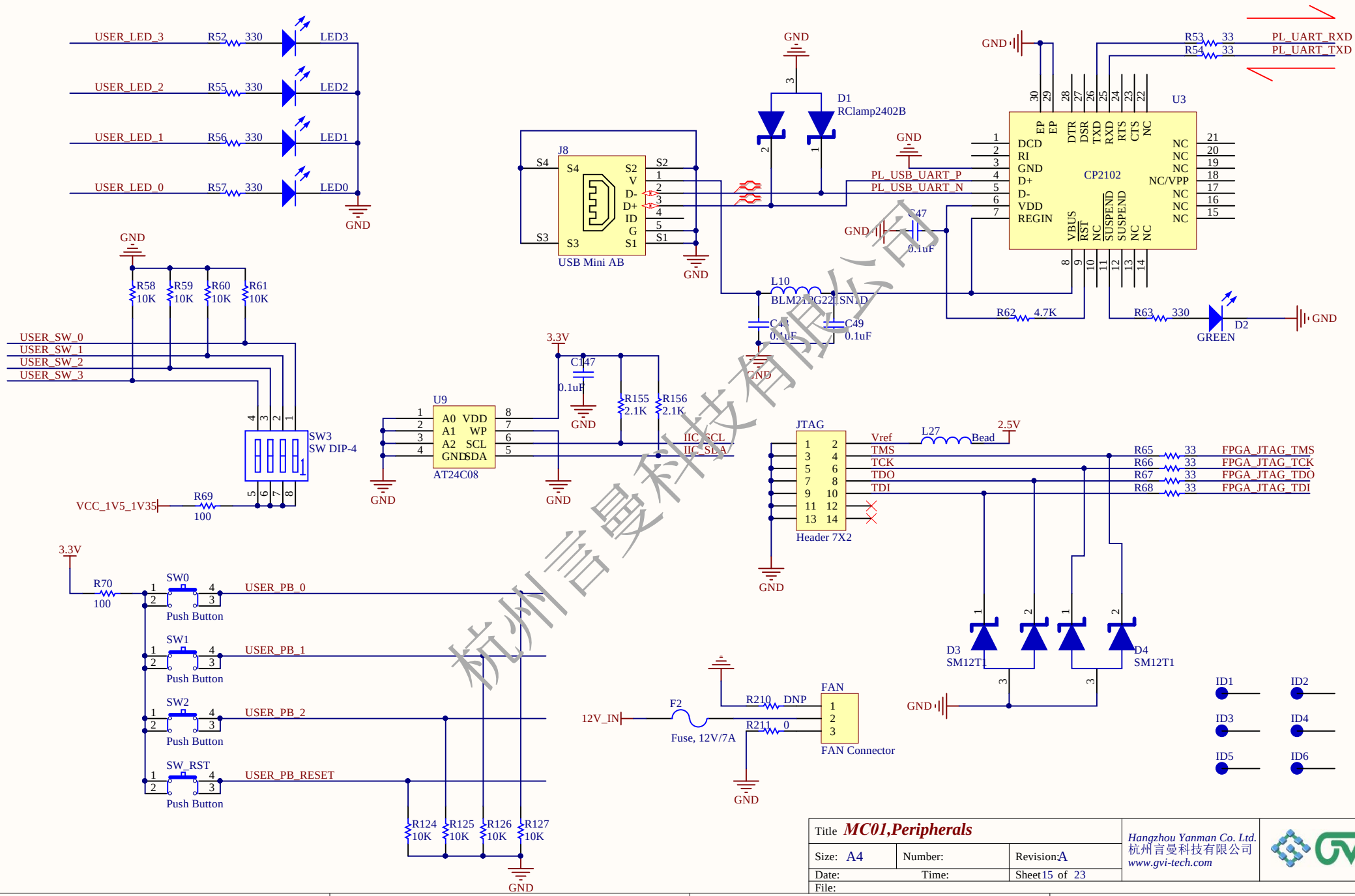
Title	*MC01,DDR3 SODIMM*		
Size: A4	Number:	Revision:A	*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Date:	Time:	Sheet12 of 23	
File:			



Title: *MC01,PCIe Gen2 X8*		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A
Date:	Time:	Sheet 13 of 23
File:		

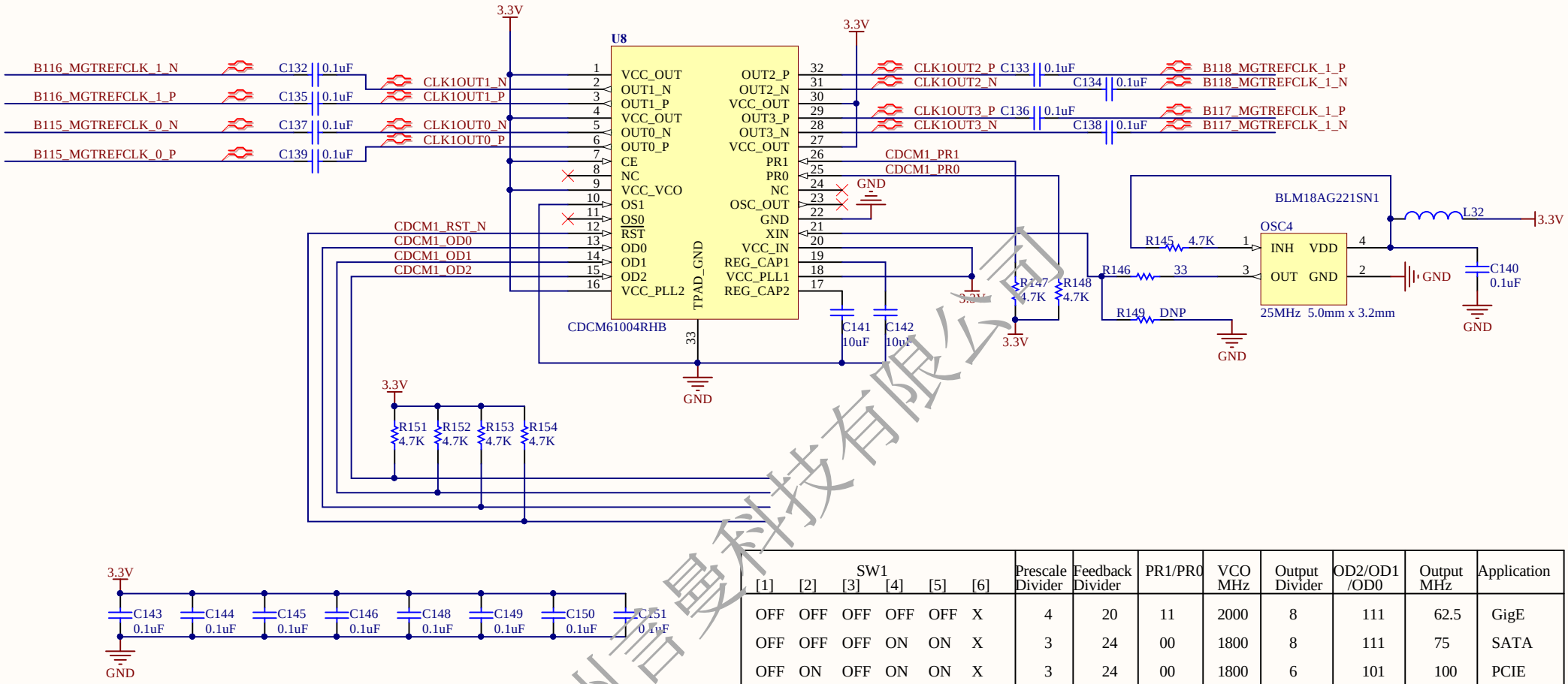


Title	*MC01, BPI Flash*		
Size: A4	Number:	Revision:A	*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Date:	Time:	Sheet14 of 23	
File:			



Title **MC01,Peripherals**		
Size: A4	Number:	Revision:A
Date:	Time:	Sheet15 of 23
File:		

Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com

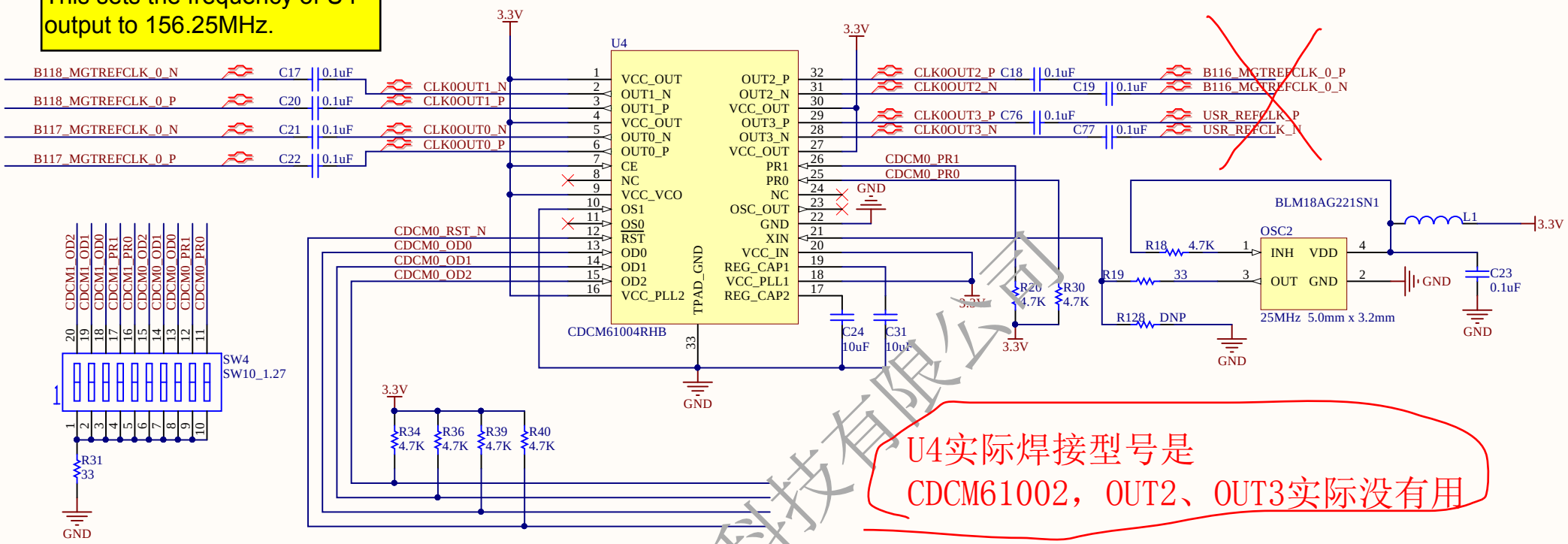


SW1 [1]	[2]	[3]	[4]	[5]	[6]	Prescale Divider	Feedback Divider	PR1/PR0	VCO MHz	Output Divider	OD2/OD1 /OD0	Output MHz	Application
OFF	OFF	OFF	OFF	OFF	X	4	20	11	2000	8	111	62.5	GigE
OFF	OFF	OFF	ON	ON	X	3	24	00	1800	8	111	75	SATA
OFF	ON	OFF	ON	ON	X	3	24	00	1800	6	101	100	PCIE
OFF	OFF	ON	OFF	OFF	X	4	20	11	2000	4	011	125	GigE
OFF	OFF	ON	ON	ON	X	3	24	00	1800	4	011	150	SATA
OFF	OFF	ON	OFF	ON	X	3	25	10	1875	4	011	156.25	10 GigE
OFF	ON	ON	ON	OFF	X	5	15	01	1875	2	001	187.5	12 GigE
ON	OFF	ON	ON	ON	X	3	24	00	1800	3	010	200	PCIE
OFF	ON	ON	OFF	OFF	X	4	20	11	2000	2	001	250	GigE
OFF	ON	ON	OFF	ON	X	3	25	10	1875	2	001	312.5	XGMII
ON	ON	ON	OFF	ON	X	3	25	10	1875	1	000	625	10 GigE

单板上U8不焊接
不需要使用

Title: MC01,Clock Generator			Hangzhou Yanman Co. Ltd. 杭州言曼科技有限公司 www.gvi-tech.com
Size: A4	Number:	Revision: A	
Date:	Time:	Sheet 16 of 23	
File:			

Set SW4 [6 to 10] to ON-OFF-OFF-OFF-ON. This sets the frequency of U4 output to 156.25MHz.

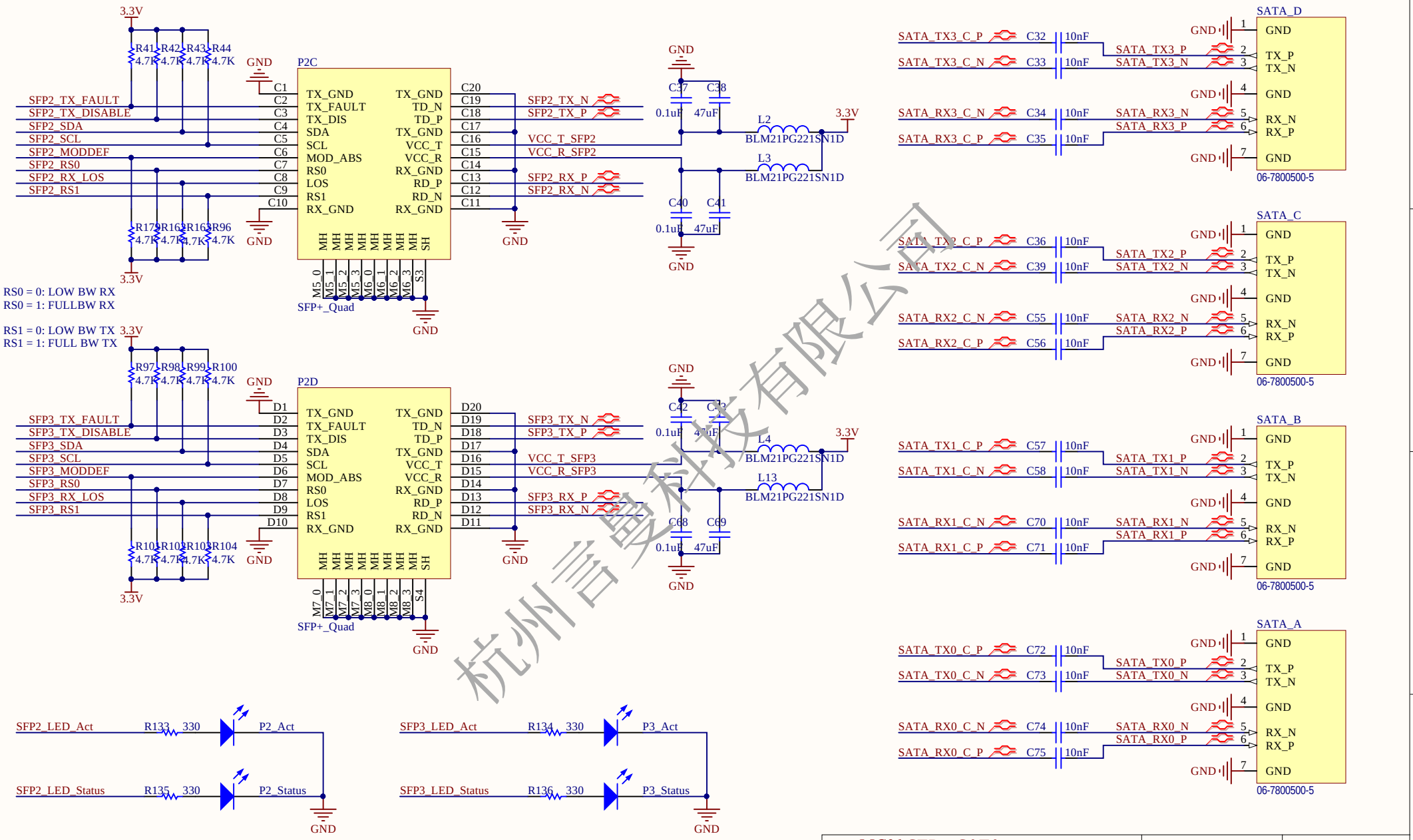


U4实际焊接型号是
CDCM61002，OUT2、OUT3实际没有用

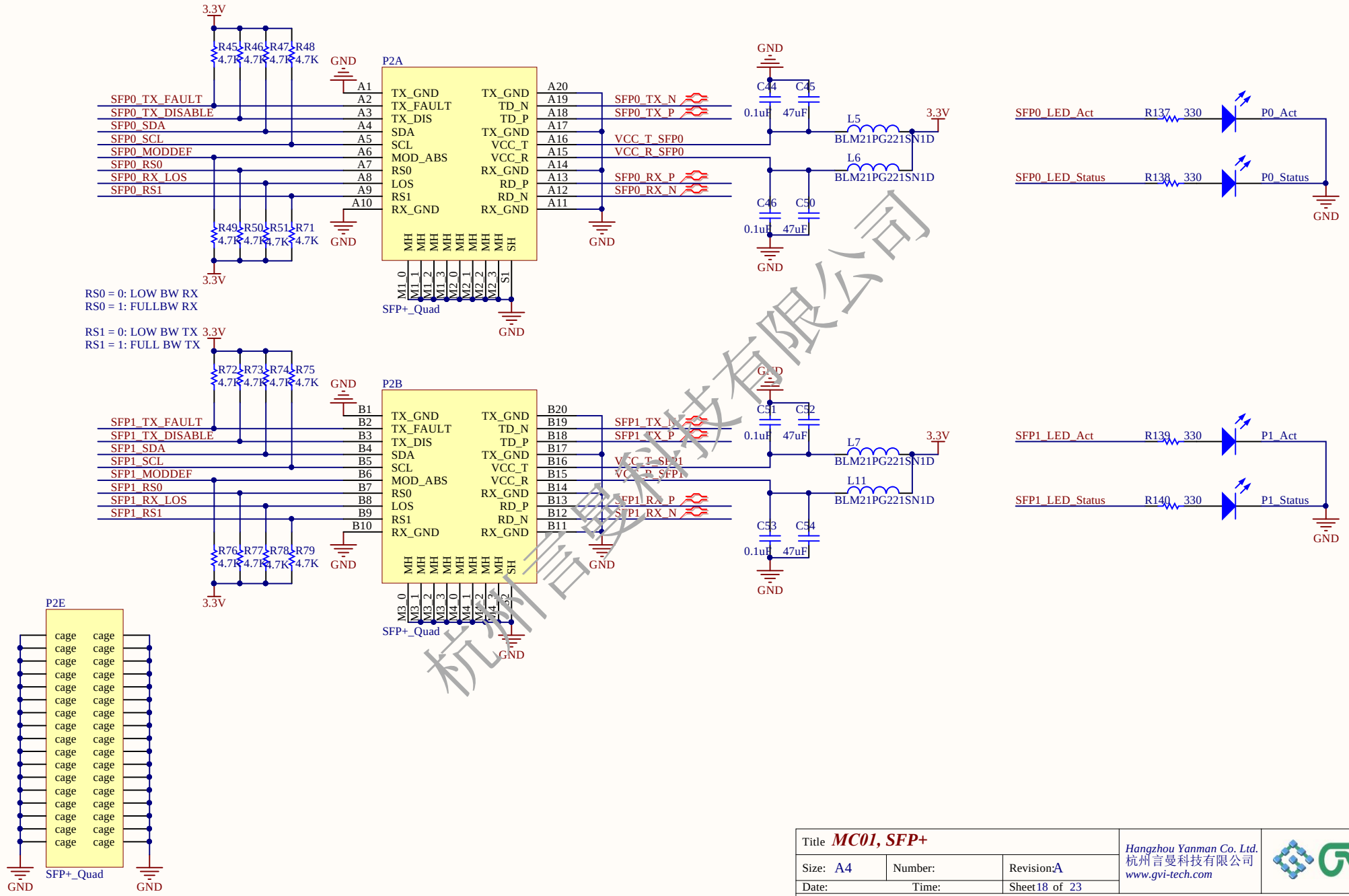
SW1 [1]	[2]	[3]	[4]	[5]	[6]	Prescale Divider	Feedback Divider	PR1/PR0	VCO MHz	Output Divider	OD2/OD1 /OD0	Output MHz	Application
OFF	OFF	OFF	OFF	OFF	X	4	20	11	2000	8	111	62.5	GigE
OFF	OFF	OFF	ON	ON	X	3	24	00	1800	8	111	75	SATA
OFF	ON	OFF	ON	ON	X	3	24	00	1800	6	101	100	PCIE
OFF	OFF	ON	OFF	OFF	X	4	20	11	2000	4	011	125	GigE
OFF	OFF	ON	ON	ON	X	3	24	00	1800	4	011	150	SATA
OFF	OFF	ON	OFF	ON	X	3	25	10	1875	4	011	156.25	10 GigE
OFF	ON	ON	ON	OFF	X	5	15	01	1875	2	001	187.5	12 GigE
ON	OFF	ON	ON	ON	X	3	24	00	1800	3	010	200	PCIE
OFF	ON	ON	OFF	OFF	X	4	20	11	2000	2	001	250	GigE
OFF	ON	ON	OFF	ON	X	3	25	10	1875	2	001	312.5	XGMII
ON	ON	ON	OFF	ON	X	3	25	10	1875	1	000	625	10 GigE

Title: MC01, Clock Generator		
Size: A4	Number:	Revision: A
Date:	Time:	Sheet 16 of 23
File:		

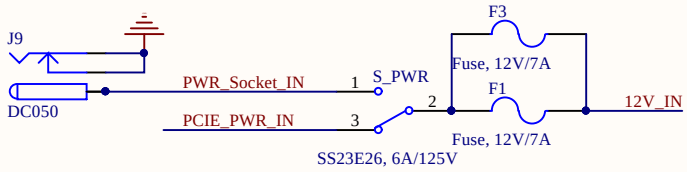
Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com



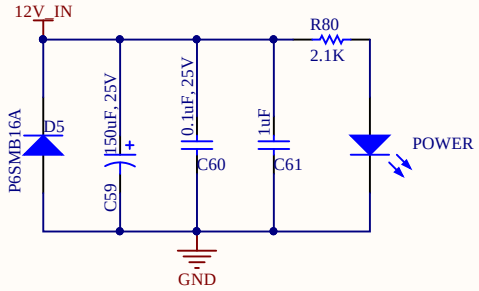
Title	*MC01,SFP+, SATA*		
Size: A4	Number:	Revision:A	*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Date:	Time:	Sheet17 of 23	
File:			



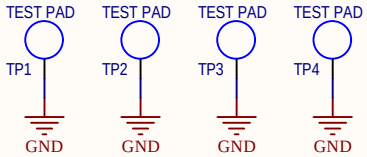
Title	***MC01, SFP+***		
Size: A4	Number:	Revision:A	*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Date:	Time:	Sheet 18 of 23	
File:			

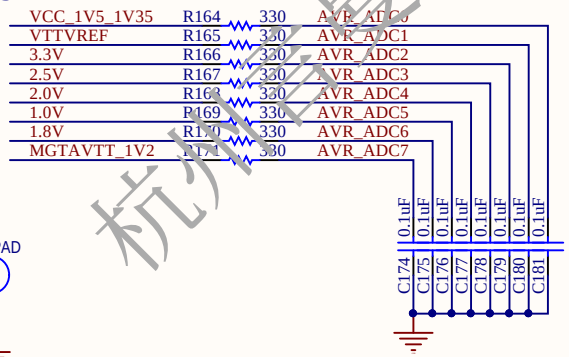


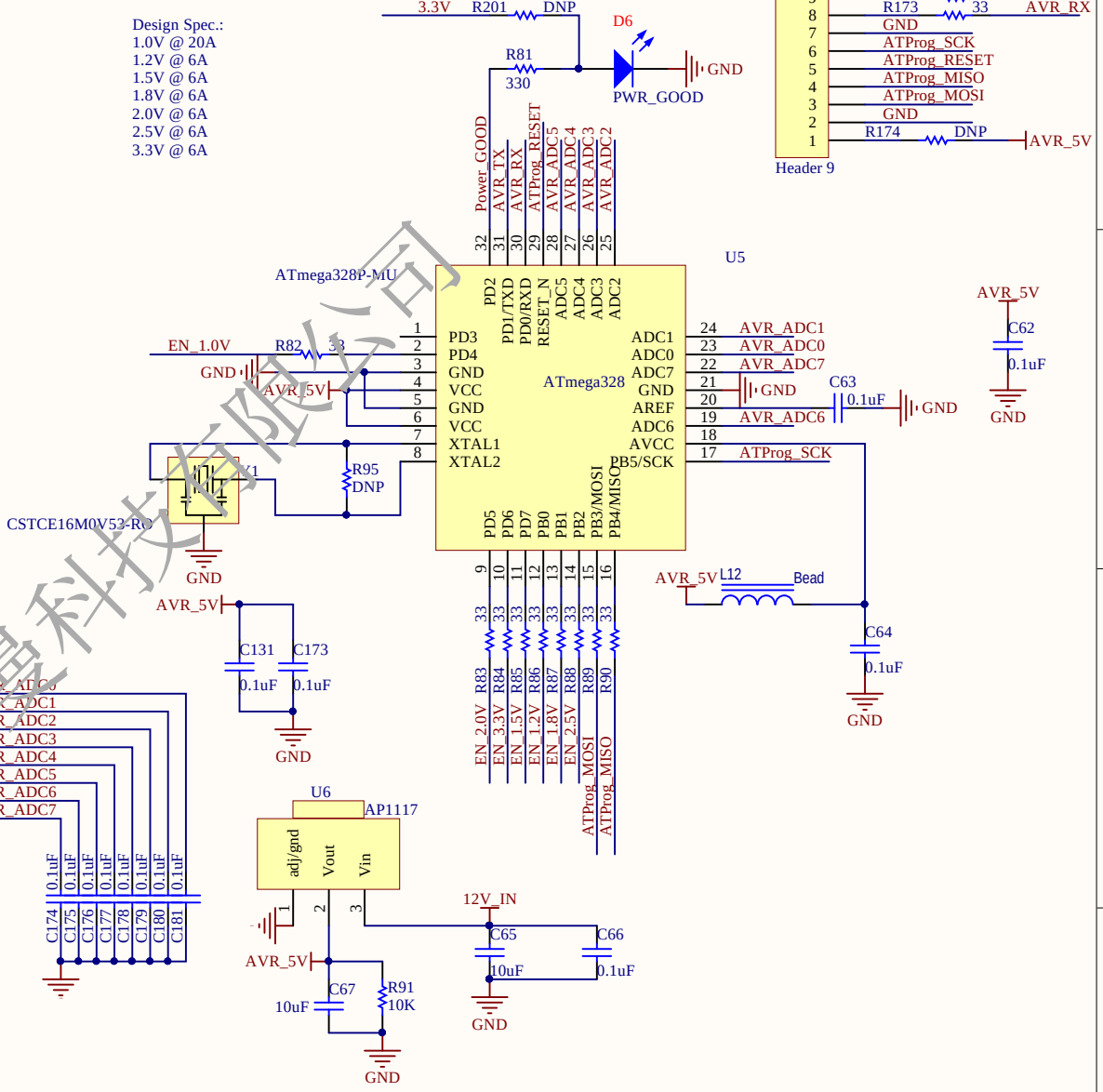
Design Spec.:
1.0V @ 20A
1.2V @ 6A
1.5V @ 6A
1.8V @ 6A
2.0V @ 6A
2.5V @ 6A
3.3V @ 6A



1.0V->"MGTAVCC","VCCINT_FPGA","VCCBRAM"
MGTAVTT_1V2
1.8V->"VCCAUX"
VCC_1V5_1V35
2.5V->"VCC2V5_FPGA","CONF_2V5"
2.0V->"VCCAUX_IO"
3.3V
VTTDDR
VTTVREF

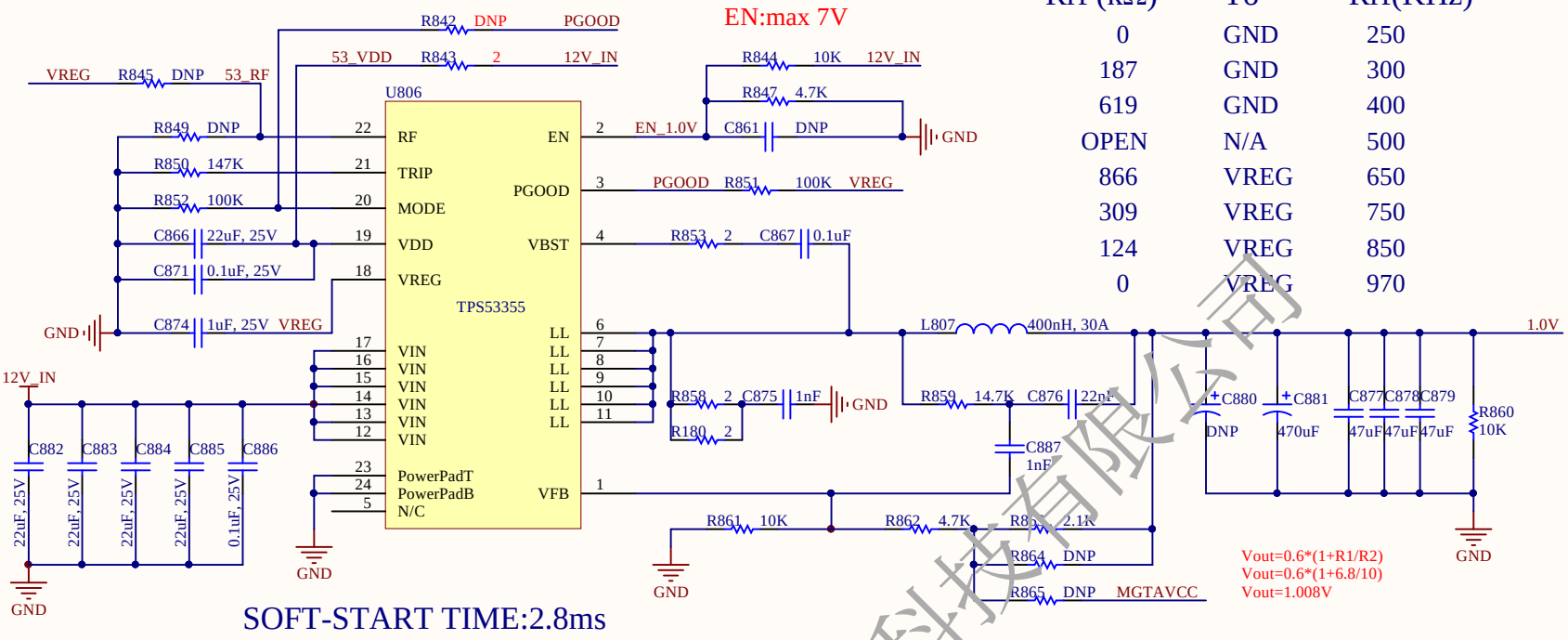






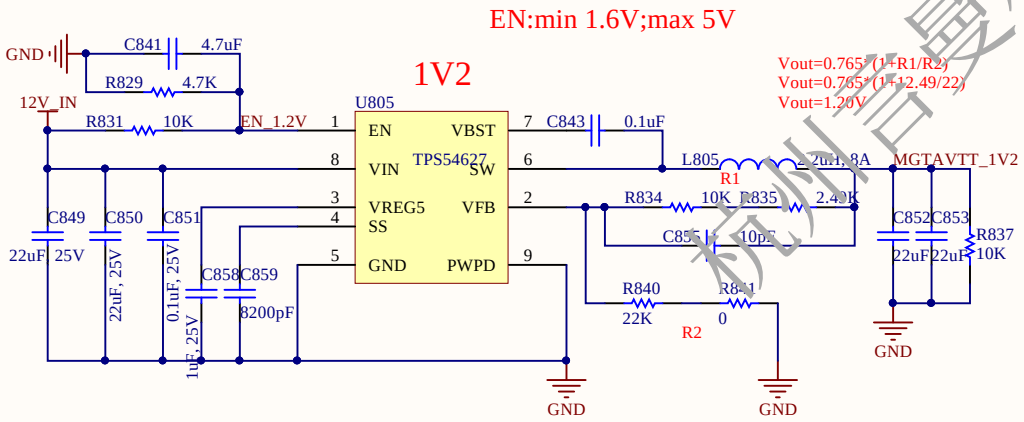
Power-On Sequence:
1.0V --> 1.8V --> 1.5V & 2.0V --> 2.5V & 3.3V --> 1.2V

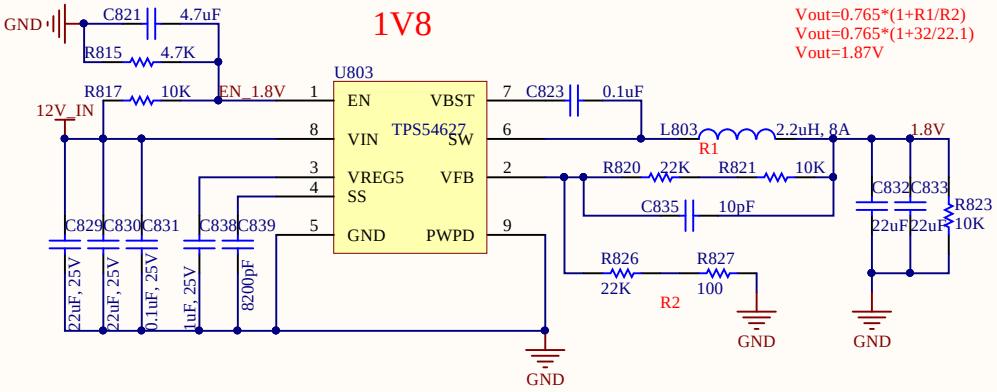
Title: *MC01,Power Management*		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A
Date:	Time:	Sheet19 of 23
File:		



Rrf (kΩ)	To	Rrf(KHz)
0	GND	250
187	GND	300
619	GND	400
OPEN	N/A	500
866	VREG	650
309	VREG	750
124	VREG	850
0	VREG	970

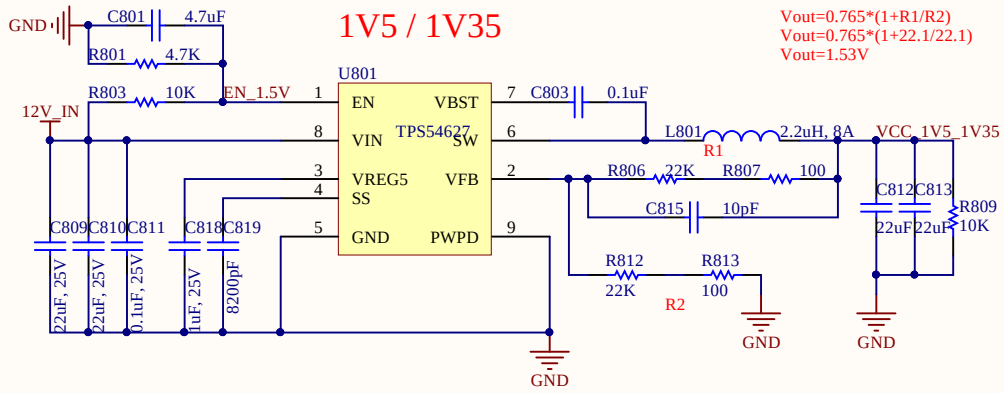
SOFT-START TIME:2.8ms

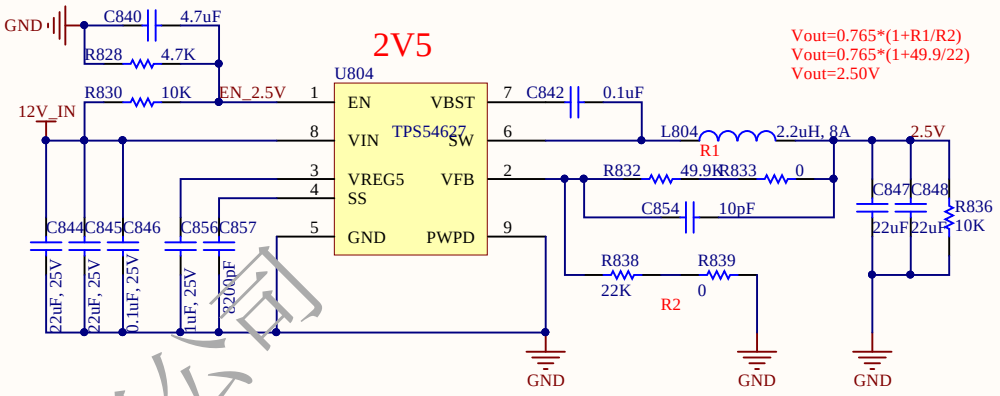


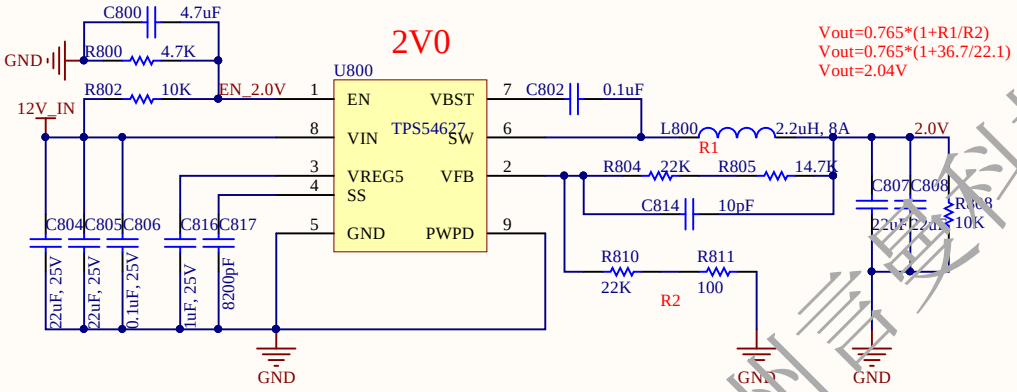


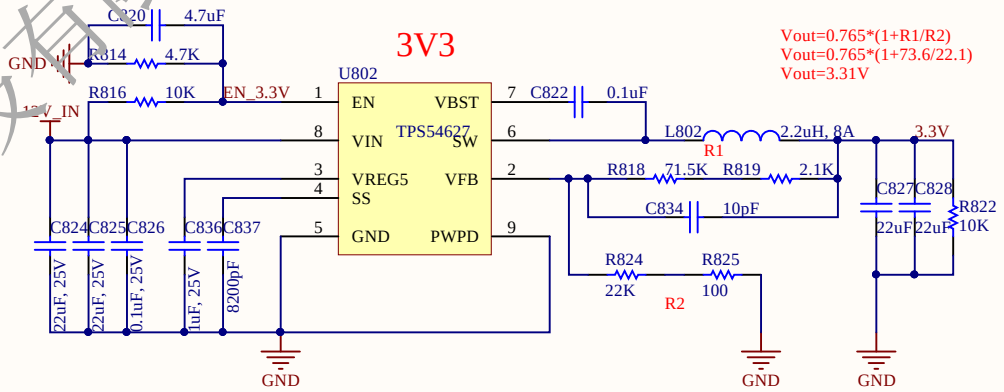
Title: *MC01, Power Suppilier*		
Size: A4	Number:	Revision: A
Date:	Time:	Sheet 20 of 23
File:		

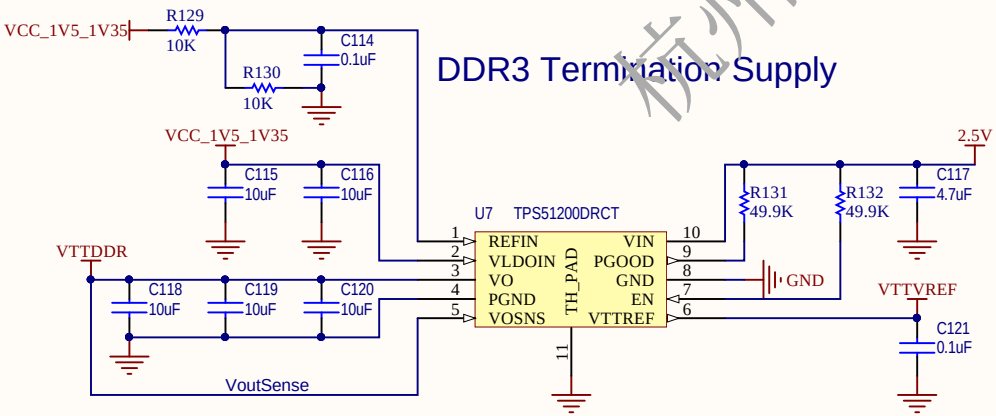
Hangzhou Yanman Co. Ltd.
杭州言曼科技有限公司
www.gvi-tech.com



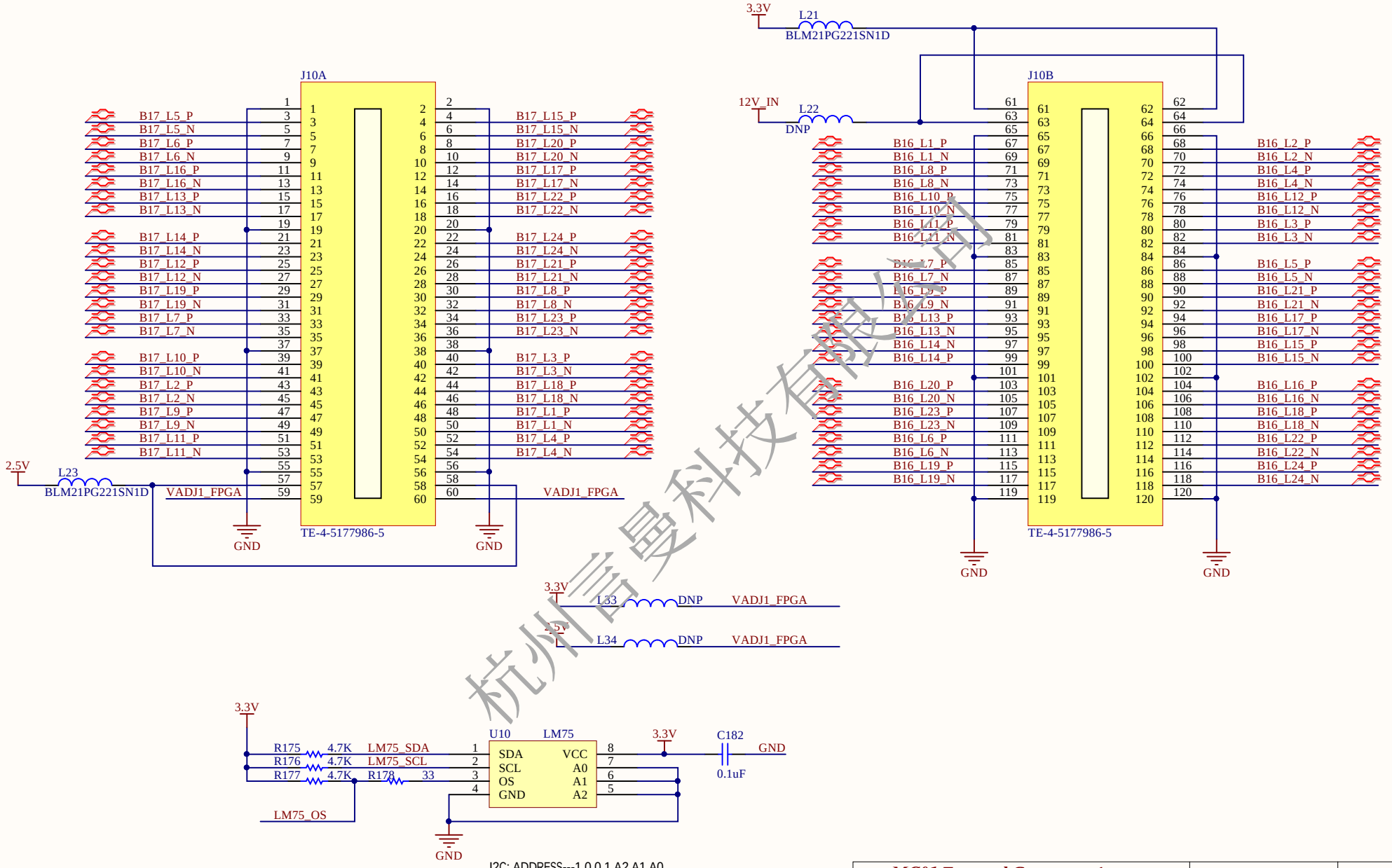




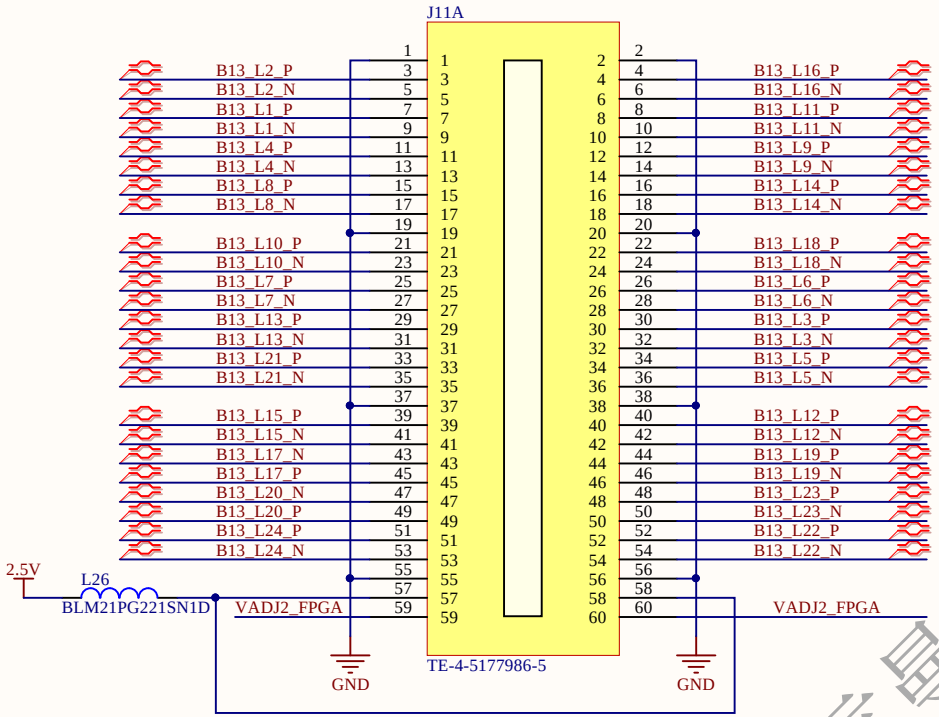


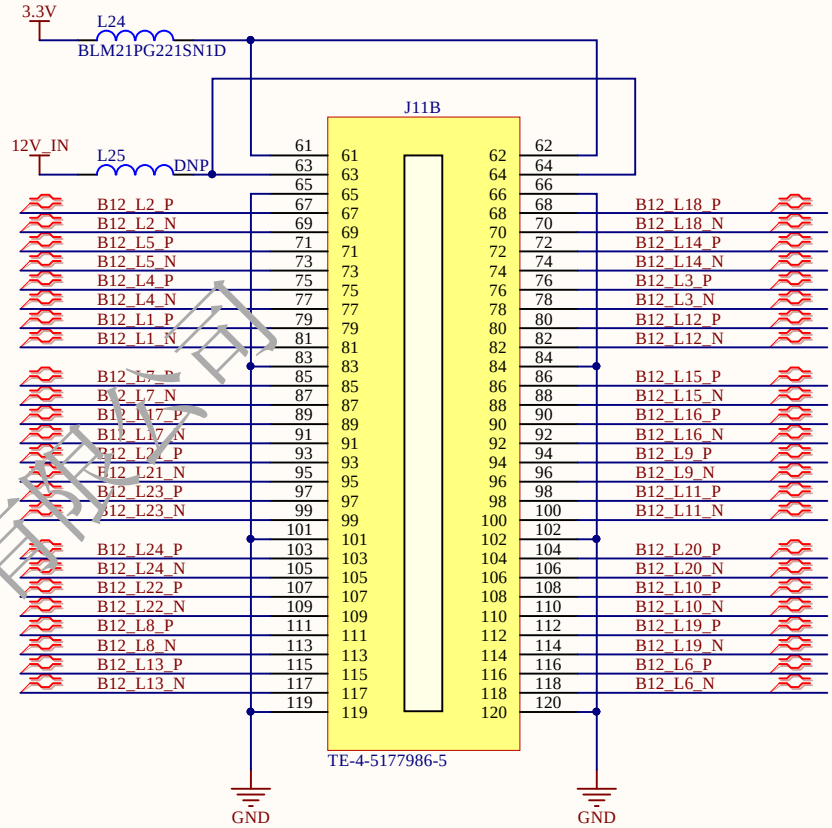


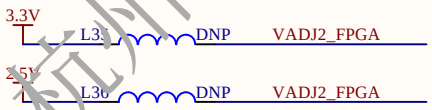
Title *MC01,Power Supplier*		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A
Date:	Time:	Sheet21 of 23
File:		



Title	***MC01,External Connector 1***		*Hangzhou Yanman Co. Ltd.* 杭州言曼科技有限公司 *www.gvi-tech.com*
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet22 of 23	
File:			







Title **MC01,External Connector 2**			Hangzhou Yanman Co. Ltd. 杭州言曼科技有限公司 www.gvi-tech.com
Size: A4	Number:	Revision:A	
Date:	Time:	Sheet23 of 23	
File:			