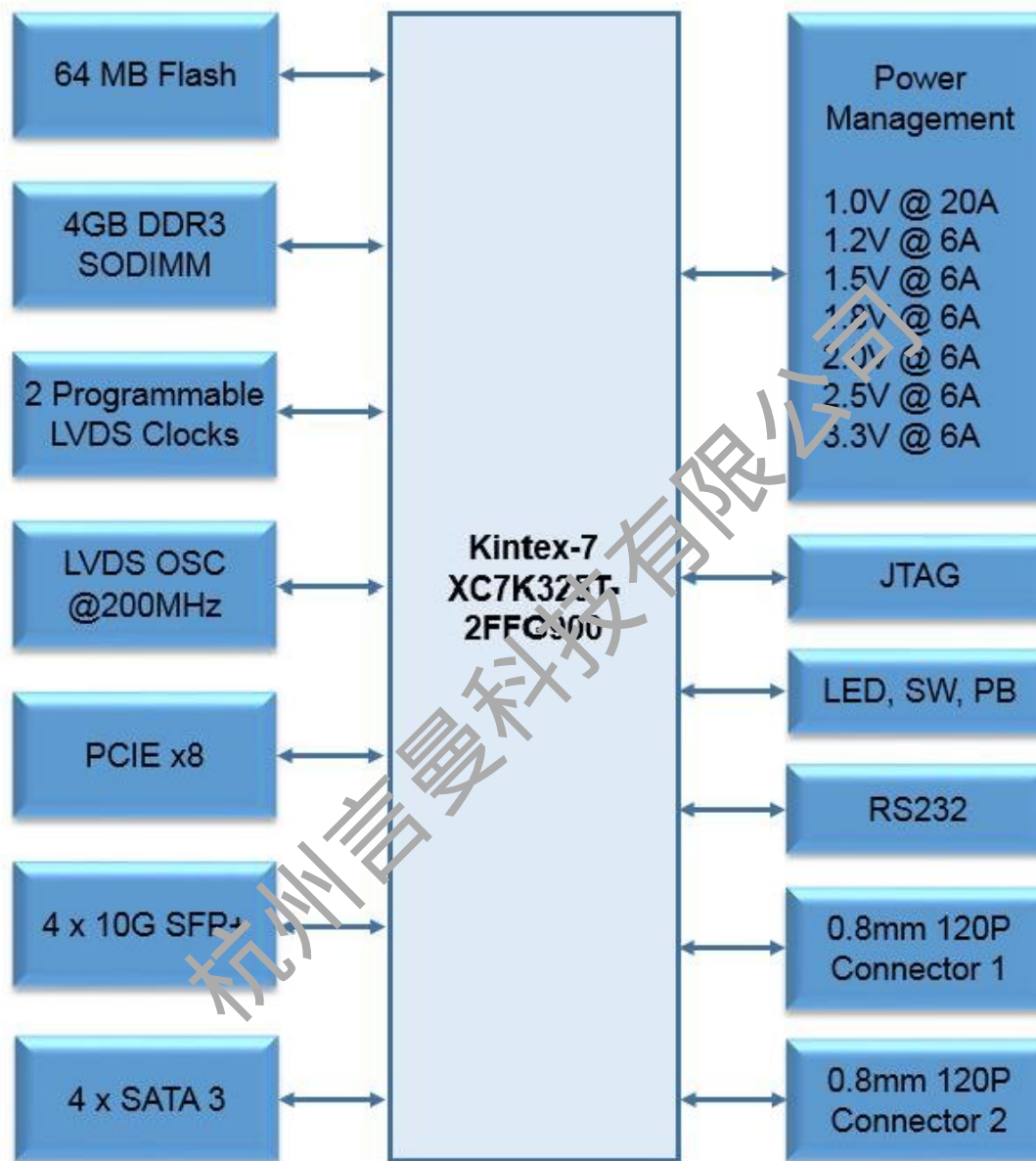


Title **MC01,Block Diagram**Size: **A4**

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U1A

BANK0

M1_0	AB2	FPGA_M1
M0_0	AB5	FPGA_M0
M2_0	AB1	FPGA_M2
DONE_0	M10	FPGA_CONF_DONE
CFGBVS_0	L10	R123 0
PROGRAM_B_0	K10	FPGA_PROG_B
INIT_B_0	A10	FLASH_Reset_N
TDI_0	H10	FPGA_JTAG_TDI
TDO_0	G10	FPGA_JTAG_TDO
TMS_0	F10	FPGA_JTAG_TMS
TCK_0	E10	FPGA_JTAG_TCK
CCLK_0	B10	Clock_to_Flash_1
VCCBATT_0	C10	AES_BATT
VN_0	T14	
VP_0	R15	
VREFP_0	T15	
VREFN_0	R14	
DXP_0	U15	
GNDADC_0	P14	
VCCADC_0	P15	
DXN_0	U14	

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FPGA_M0
FPGA_M1
FPGA_M2

7 Series FPGA Configuration Modes

Bus Width fixed in BitGen Config

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1,2,4	Output
Master BPI	010	8,16	Output
Master SelectMAP	100	8,16	Output
JTAG	101	1	Not Applicable
Slave SelectMAP	110	8,16,32	Input
Slave serial	111	1	Input

VCC2V5_FPGA

R141

4.7K

PROG_B

Push Button

GND

C267

0.1uF

GND

L14

BLM15AG121SN1D

1.8V

C78

0.1uF

GNDADC

From 2.5V
VCC2V5_FPGA

FPGA_CONF_DONE

R35

0

DONE

R38

330

GND

VADJ2_FPGA

Y22

AK22

AG21

AF24

AD20

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

VCCO_12

U1B

BANK12

IO_25_12	AE20	
IO_L24N_T3_12	AK21	B12_L24_N
IO_L24P_T3_12	AK20	B12_L24_P
IO_L23N_T3_12	AJ21	B12_L23_N
IO_L23P_T3_12	AH21	B12_L23_P
IO_L22N_T3_12	AH20	B12_L22_N
IO_L22P_T3_12	AG20	B12_L22_P
IO_L21N_T3_DQS_12	AJ23	B12_L21_N
IO_L21P_T3_DQS_12	AJ22	B12_L21_P
IO_L20N_T3_12	AH22	B12_L20_N
IO_L20P_T3_12	AG22	B12_L20_P
IO_L19N_T3_VREF_12	AF21	B12_L19_N
IO_L19P_T3_12	AF20	B12_L19_P
IO_L18N_T2_12	AH25	B12_L18_N
IO_L18P_T2_12	AG25	B12_L18_P
IO_L17N_T2_12	AK24	B12_L17_N
IO_L17P_T2_12	AK23	B12_L17_P
IO_L16N_T2_12	AF25	B12_L16_N
IO_L16P_T2_12	AE25	B12_L16_P
IO_L15N_T2_DQS_12	AK25	B12_L15_N
IO_L15P_T2_DQS_12	AJ24	B12_L15_P
IO_L14N_T2_SRCC_12	AH24	B12_L14_N
IO_L14P_T2_SRCC_12	AG24	B12_L14_P
IO_L13N_T2_MRCC_12	AF22	B12_L13_N
IO_L13P_T2_MRCC_12	AE24	B12_L13_P
IO_L12N_T1_MRCC_12	AD23	B12_L12_N
IO_L12P_T1_MRCC_12	AF23	B12_L12_P
IO_L11N_T1_SRCC_12	AE23	B12_L11_N
IO_L11P_T1_SRCC_12	AE21	B12_L11_P
IO_L10N_T1_12	AD21	B12_L10_N
IO_L10P_T1_12	AD24	B12_L10_P
IO_L9N_T1_DQS_12	AC24	B12_L9_N
IO_L9P_T1_DQS_12	AD22	B12_L9_P
IO_L8N_T1_12	AC22	B12_L8_N
IO_L8P_T1_12	AC25	B12_L8_P
IO_L7N_T1_12	AB24	B12_L7_N
IO_L7P_T1_12	AB20	B12_L7_P
IO_L6N_T0_VREF_12	AA20	B12_L6_N
IO_L6P_T0_12	AC21	B12_L6_P
IO_L5N_T0_12	AC20	B12_L5_N
IO_L5P_T0_12	AA23	B12_L5_P
IO_L4N_T0_12	AA22	B12_L4_N
IO_L4P_T0_12	AB23	B12_L4_P
IO_L3N_T0_DQS_12	AB22	B12_L3_N
IO_L3P_T0_DQS_12	AA21	B12_L3_P
IO_L2N_T0_12	Y21	B12_L2_N
IO_L2P_T0_12	Y24	B12_L2_P
IO_L1N_T0_12	Y23	B12_L1_N
IO_L1P_T0_12	Y20	B12_L1_P
IO_0_12		

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In order to avoid voltage level mismatch,
VADJ2_FPGA must be supplied by external module.

Title MC01,Bank 0, 12

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U1C

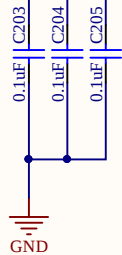
BANK13

IO_25_13	AE26
IO_L24N_T3_13	AK26 B13 L24 N
IO_L24P_T3_13	AJ26 B13 L24 P
IO_L23N_T3_13	AF27 B13 L23 N
IO_L23P_T3_13	AF26 B13 L23 P
IO_L22N_T3_13	AH27 B13 L22 N
IO_L22P_T3_13	AH26 B13 L22 P
IO_L21N_T3_DQS_13	AG28 B13 L21 N
IO_L21P_T3_DQS_13	AG27 B13 L21 P
IO_L20N_T3_13	AK28 B13 L20 N
IO_L20P_T3_13	AJ27 B13 L20 P
IO_L19N_T3_VREF_13	AD26 B13 L19 N
IO_L19P_T3_13	AC26 B13 L19 P
IO_L18N_T2_13	AH30 B13 L18 N
IO_L18P_T2_13	AG30 B13 L18 P
IO_L17N_T2_13	AJ29 B13 L17 N
IO_L17P_T2_13	AJ28 B13 L17 P
IO_L16N_T2_13	AF30 B13 L16 N
IO_L16P_T2_13	AE30 B13 L16 P
IO_L15N_T2_DQS_13	AK30 B13 L15 N
IO_L15P_T2_DQS_13	AK29 B13 L15 P
IO_L14N_T2_SRCC_13	AF28 B13 L14 N
IO_L14P_T2_SRCC_13	AE28 B13 L14 P
IO_L13N_T2_MRCC_13	AH29 B13 L13 N
IO_L13P_T2_MRCC_13	AG29 B13 L13 P
IO_L12N_T1_MRCC_13	AC27 B13 L12 N
IO_L12P_T1_MRCC_13	AB27 B13 L12 P
IO_L11N_T1_SRCC_13	AD28 B13 L11 N
IO_L11P_T1_SRCC_13	AD27 B13 L11 P
IO_L10N_T1_13	AB30 B13 L10 N
IO_L10P_T1_13	AB29 B13 L10 P
IO_L9N_T1_DQS_13	AE29 B13 L9 N
IO_L9P_T1_DQS_13	AD29 B13 L9 P
IO_L8N_T1_13	AA30 B13 L8 N
IO_L8P_T1_13	Y30 B13 L8 P
IO_L7N_T1_13	AC30 B13 L7 N
IO_L7P_T1_13	AC29 B13 L7 P
IO_L6N_T0_VREF_13	AB25 B13 L6 N
IO_L6P_T0_13	AA25 B13 L6 P
IO_L5N_T0_13	AB28 B13 L5 N
IO_L5P_T0_13	AA27 B13 L5 P
IO_L4N_T0_13	Y29 B13 L4 N
IO_L4P_T0_13	W29 B13 L4 P
IO_L3N_T0_DQS_13	AA28 B13 L3 N
IO_L3P_T0_DQS_13	Y28 B13 L3 P
IO_L2N_T0_13	W28 B13 L2 N
IO_L2P_T0_13	W27 B13 L2 P
IO_L1N_T0_13	AA26 B13 L1 N
IO_L1P_T0_13	Y26 B13 L1 P
IO_0_13	Y25

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VADJ2_FPGA

AJ25	VCCO_13
AH28	VCCO_13
AE27	VCCO_13
AD30	VCCO_13
AB26	VCCO_13
AA29	VCCO_13



U1D

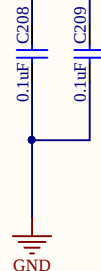
BANK14

IO_25_14	W19
IO_L24N_T3_A00_D16_14	W22 FLASH A0
IO_L24P_T3_A01_D17_14	W21 FLASH A1
IO_L23N_T3_A02_D18_14	V24 FLASH A2
IO_L23P_T3_A03_D19_14	U24 FLASH A3
IO_L22N_T3_A04_D20_14	V22 FLASH A4
IO_L22P_T3_A05_D21_14	V21 FLASH A5
IO_L21N_T3_DQS_A06_D22_14	U23 FLASH A6
IO_L21P_T3_DQS_14	U22
IO_L20N_T3_A07_D23_14	W24 FLASH A7
IO_L20P_T3_A08_D24_14	W23 FLASH A8
IO_L19N_T3_A09_D25_VREF_14	V20 FLASH A9
IO_L19P_T3_A10_D26_14	V19 FLASH A10
IO_L18N_T2_A11_D27_14	W26 FLASH A11
IO_L18P_T2_A12_D28_14	V25 FLASH A12
IO_L17N_T2_A13_D29_14	V30 FLASH A13
IO_L17P_T2_A14_D30_14	V29 FLASH A14
IO_L16N_T2_A15_D31_14	V27 FLASH A15
IO_L16P_T2_CSI_B_14	V26
IO_L15N_T2_DQS_DOUT_CSO_14	U30
IO_L15P_T2_DQS_RDWR_B_1_14	U29 FLASH WAIT
IO_L14N_T2_SRCC_14	U25
IO_L14P_T2_SRCC_14	T25
IO_L13N_T2_MRCC_14	U28
IO_L13P_T2_MRCC_14	U27
IO_L12N_T1_MRCC_14	T27
IO_L12P_T1_MRCC_14	T26
IO_L11N_T1_SRCC_14	T28
IO_L11P_T1_SRCC_14	R28
IO_L10N_T1_D15_14	R26 FLASH D15
IO_L10P_T1_D14_14	P26 FLASH D14
IO_L9N_T1_DQS_D13_14	T30 FLASH D13
IO_L9P_T1_DQS_14	R30
IO_L8N_T1_D12_14	P28 FLASH D12
IO_L8P_T1_D11_14	P27 FLASH D11
IO_L7N_T1_D10_14	R29 FLASH D10
IO_L7P_T1_D09_14	P29 FLASH D9
IO_L6N_T0_D08_VREF_14	U20 FLASH D8
IO_L6P_T0_FCS_B_14	U19 FLASH CE_N
IO_L5N_T0_D07_14	T23 FLASH D7
IO_L5P_T0_D06_14	T22 FLASH D6
IO_L4N_T0_D05_14	T21 FLASH D5
IO_L4P_T0_D04_14	T20 FLASH D4
IO_L3N_T0_DQS_EMCCCLK_14	R24 EMCCCLK
IO_L3P_T0_DQS_PUDC_B_14	R23
IO_L2N_T0_D03_14	R21 FLASH D3
IO_L2P_T0_D02_14	R20 FLASH D2
IO_L1N_T0_D01_DIN_14	R25 FLASH D1
IO_L1P_T0_D00_MOSI_14	P24 FLASH D0
IO_0_14	R19

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From 2.5V
VCC2V5_FPGA

W25	VCCO_14
V28	VCCO_14
U21	VCCO_14
T24	VCCO_14
R27	VCCO_14
P30	VCCO_14



Title MC01,Bank 13, 14

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U1E

BANK15

IO_25_15
IO_L24N_T3_RS0_15
IO_L24P_T3_RS1_15
IO_L23N_T3_FWE_B_15
IO_L23P_T3_FOE_B_15
IO_L22N_T3_A16_15
IO_L22P_T3_A17_15
IO_L21N_T3_DQS_A18_15
IO_L21P_T3_DQS_15
IO_L20N_T3_A19_15
IO_L20P_T3_A20_15
IO_L19N_T3_A21_VREF_15
IO_L19P_T3_A22_15
IO_L18N_T2_A23_15
IO_L18P_T2_A24_15
IO_L17N_T2_A25_15
IO_L17P_T2_A26_15
IO_L16N_T2_A27_15
IO_L16P_T2_A28_15
IO_L15N_T2_DQS_ADV_B_15
IO_L15P_T2_DQS_15
IO_L14N_T2_SRCC_15
IO_L14P_T2_SRCC_15
IO_L13N_T2_MRCC_15
IO_L13P_T2_MRCC_15
IO_L12N_T1_MRCC_AD5N_15
IO_L12P_T1_MRCC_AD5P_15
IO_L11N_T1_SRCC_AD12N_1
IO_L11P_T1_SRCC_AD12P_1
IO_L10N_T1_AD4N_15
IO_L10P_T1_AD4P_15
IO_L9N_T1_DQS_AD11N_15
IO_L9P_T1_DQS_AD11P_15
IO_L8N_T1_AD3N_15
IO_L8P_T1_AD3P_15
IO_L7N_T1_AD10N_15
IO_L7P_T1_AD10P_15
IO_L6N_T0_VREF_15
IO_L6P_T0_15
IO_L5N_T0_AD2N_15
IO_L5P_T0_AD2P_15
IO_L4N_T0_AD9N_15
IO_L4P_T0_AD9P_15
IO_L3N_T0_DQS_AD1N_15
IO_L3P_T0_DQS_AD1P_15
IO_L2N_T0_AD8N_15
IO_L2P_T0_AD8P_15
IO_L1N_T0_AD0N_15
IO_L1P_T0_AD0P_15
IO_0_15

P19 ✕
M23 ✕ FLASH_A24
M22 ✕ FLASH_A25
M25 ✕ FLASH_WE_N
M24 ✕ FLASH_OE_N
P22 ✕ FLASH_A16
P21 ✕ FLASH_A17
N24 ✕ FLASH_A18
P23 ✕
N22 ✕ FLASH_A19
N21 ✕ FLASH_A20
N20 ✕ FLASH_A21
N19 ✕ FLASH_A22
N26 ✕ FLASH_A23
N25 ✕
N30 ✕ R204 DNP
N29 ✕
M27 ✕
N27 ✕
M30 ✕ FLASH_ADV_N
M29 ✕
L28 ✕
M28 ✕
K29 ✕ R205 DNP
K28 ✕
K25 ✕ USR_REFCLK_N
L25 ✕ USR_REFCLK_P
L27 ✕
L26 ✕
J26 ✕
K26 ✕
K30 ✕ R202 DNP
L30 ✕ R203 DNP
J28 ✕
J27 ✕
H29 ✕
J29 ✕
L20 ✕ SFP0_LED_Act
M20 ✕ SFP0_LED_Status
J22 ✕ SFP1_LED_Act
J21 ✕ SFP1_LED_Status
K21 ✕ SFP2_LED_Act
L21 ✕ SFP2_LED_Status
K24 ✕ SFP3_LED_Act
K23 ✕ SFP3_LED_Status
L23 ✕
L22 ✕
J24 ✕
M24 ✕
M25 ✕

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BANK16

IO_25_16
IO_L24N_T3_16
IO_L24P_T3_16
IO_L23N_T3_16
IO_L23P_T3_16
IO_L22N_T3_16
IO_L22P_T3_16
IO_L21N_T3_DQS_16
IO_L21P_T3_DQS_16
IO_L20N_T3_16
IO_L20P_T3_16
IO_L19N_T3_VREF_16
IO_L19P_T3_16
IO_L18N_T2_16
IO_L18P_T2_16
IO_L17N_T2_16
IO_L17P_T2_16
IO_L16N_T2_16
IO_L16P_T2_16
IO_L15N_T2_DQS_16
IO_L15P_T2_DQS_16
IO_L14N_T2_SRCC_16
IO_L14P_T2_SRCC_16
IO_L13N_T2_MRCC_16
IO_L13P_T2_MRCC_16
IO_L12N_T1_MRCC_16
IO_L12P_T1_MRCC_16
IO_L11N_T1_SRCC_16
IO_L11P_T1_SRCC_16
IO_L10N_T1_16
IO_L10P_T1_16
IO_L9N_T1_DQS_16
IO_L9P_T1_DQS_16
IO_L8N_T1_16
IO_L8P_T1_16
IO_L7N_T1_16
IO_L7P_T1_16
IO_L6N_T0_VREF_16
IO_L6P_T0_16
IO_L5N_T0_16
IO_L5P_T0_16
IO_L4N_T0_16
IO_L4P_T0_16
IO_L3N_T0_DQS_16
IO_L3P_T0_DQS_16
IO_L2N_T0_16
IO_L2P_T0_16
IO_L1N_T0_16
IO_L1P_T0_16
IO_0_16

G25
G30 B16_L24_N
H30 B16_L24_P
H27 B16_L23_N
H26 B16_L23_P
F30 B16_L22_N
G29 B16_L22_P
F27 B16_L21_N
G27 B16_L21_P
F28 B16_L20_N
G28 B16_L20_P
H25 B16_L19_N
H24 B16_L19_P
E30 B16_L18_N
E29 B16_L18_P
A30 B16_L17_N
B30 B16_L17_P
C30 B16_L16_N
D29 B16_L16_P
B29 B16_L15_N
C29 B16_L15_P
D28 B16_L14_N
E28 B16_L14_P
C27 B16_L13_N
D27 B16_L13_P
B25 B16_L12_N
C25 B16_L12_P
C26 B16_L11_N
D26 B16_L11_P
A26 B16_L10_N
A25 B16_L10_P
A28 B16_L9_N
B28 B16_L9_P
B24 B16_L8_N
C24 B16_L8_P
A27 B16_L7_N
B27 B16_L7_P
G24 B16_L6_N
G23 B16_L6_P
E26 B16_L5_N
F26 B16_L5_P
D24 B16_L4_N
E24 B16_L4_P
E25 B16_L3_N
F25 B16_L3_P
D23 B16_L2_N
E23 B16_L2_P
A23 B16_L1_N
B23 B16_L1_P
F23

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VADJ1_FPGA

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U1G

BANK17

IO_25_17
IO_L24N_T3_17
IO_L24P_T3_17
IO_L23N_T3_17
IO_L23P_T3_17
IO_L22N_T3_17
IO_L22P_T3_17
IO_L21N_T3_DQS_17
IO_L21P_T3_DQS_17
IO_L20N_T3_17
IO_L20P_T3_17
IO_L19N_T3_VREF_17
IO_L19P_T3_17
IO_L18N_T2_17
IO_L18P_T2_17
IO_L17N_T2_17
IO_L17P_T2_17
IO_L16N_T2_17
IO_L16P_T2_17
IO_L15N_T2_DQS_17
IO_L15P_T2_DQS_17
IO_L14N_T2_SRCC_17
IO_L14P_T2_SRCC_17
IO_L13N_T2_MRCC_17
IO_L13P_T2_MRCC_17
IO_L12N_T1_MRCC_17
IO_L12P_T1_MRCC_17
IO_L11N_T1_SRCC_17
IO_L11P_T1_SRCC_17
IO_L10N_T1_17
IO_L10P_T1_17
IO_L9N_T1_DQS_17
IO_L9P_T1_DQS_17
IO_L8N_T1_17
IO_L8P_T1_17
IO_L7N_T1_17
IO_L7P_T1_17
IO_L6N_T0_VREF_17
IO_L6P_T0_17
IO_L5N_T0_17
IO_L5P_T0_17
IO_L4N_T0_17
IO_L4P_T0_17
IO_L3N_T0_DQS_17
IO_L3P_T0_DQS_17
IO_L2N_T0_17
IO_L2P_T0_17
IO_L1N_T0_17
IO_L1P_T0_17
IO_0_17

E18
B19
C19
A22
B22
A18
B18
A21
A20
A17
A16
B20
C20
F17
G17
B17
C17
F18
G18
C16
D16
D19
E19
D18
D17
E20
F20
E21
F21
C22
D22
F22
G22
C21
D21
H22
H21
K20
K19
L18
L17
H19
J19
H17
J17
G20
H20
J18
K18
G19

B17 L24 N
B17 L24 P
B17 L23 N
B17 L23 P
B17 L22 N
B17 L22 P
B17 L21 N
B17 L21 P
B17 L20 N
B17 L20 P
B17 L19 N
B17 L19 P
B17 L18 N
B17 L18 P
B17 L17 N
B17 L17 P
B17 L16 N
B17 L16 P
B17 L15 N
B17 L15 P
B17 L14 N
B17 L14 P
B17 L13 N
B17 L13 P
B17 L12 N
B17 L12 P
B17 L11 N
B17 L11 P
B17 L10 N
B17 L10 P
B17 L9 N
B17 L9 P
B17 L8 N
B17 L8 P
B17 L7 N
B17 L7 P
B17 L6 N
B17 L6 P
B17 L5 N
B17 L5 P
B17 L4 N
B17 L4 P
B17 L3 N
B17 L3 P
B17 L2 N
B17 L2 P
B17 L1 N
B17 L1 P
B17 L0 N
B17 L0 P

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In order to avoid voltage level mismatch,
VADJ1_FPGA must be supplied by external module.

U1H

BANK18

IO_25_18
IO_L24N_T3_18
IO_L24P_T3_18
IO_L23N_T3_18
IO_L23P_T3_18
IO_L22N_T3_18
IO_L22P_T3_18
IO_L21N_T3_DQS_18
IO_L21P_T3_DQS_18
IO_L20N_T3_18
IO_L20P_T3_18
IO_L19N_T3_VREF_18
IO_L19P_T3_18
IO_L18N_T2_18
IO_L18P_T2_18
IO_L17N_T2_18
IO_L17P_T2_18
IO_L16N_T2_18
IO_L16P_T2_18
IO_L15N_T2_DQS_18
IO_L15P_T2_DQS_18
IO_L14N_T2_SRCC_18
IO_L14P_T2_SRCC_18
IO_L13N_T2_MRCC_18
IO_L13P_T2_MRCC_18
IO_L12N_T1_MRCC_18
IO_L12P_T1_MRCC_18
IO_L11N_T1_SRCC_18
IO_L11P_T1_SRCC_18
IO_L10N_T1_18
IO_L10P_T1_18
IO_L9N_T1_DQS_18
IO_L9P_T1_DQS_18
IO_L8N_T1_18
IO_L8P_T1_18
IO_L7N_T1_18
IO_L7P_T1_18
IO_L6N_T0_VREF_18
IO_L6P_T0_18
IO_L5N_T0_18
IO_L5P_T0_18
IO_L4N_T0_18
IO_L4P_T0_18
IO_L3N_T0_DQS_18
IO_L3P_T0_DQS_18
IO_L2N_T0_18
IO_L2P_T0_18
IO_L1N_T0_18
IO_L1P_T0_18
IO_0_18

F16
A15
B14
B15
C15
A13
B13
C14
D14
E15
E14
E16
F15
C11
D11
A12
A11
E11
F11
B12
C12
E13
F12
D13
D12
F13
G13
G14
H14
H12
H11
H16
J16
J12
J11
G15
H15
K11
L11
J14
K14
J13
K13
L13
L12
K15
L15
K16
L16
G12

PL UART_RXD
SFP0_TX_DISABLE
SFP1_SDA
SFP0_TX_FAULT
SFP0_SDA
SFP1_SCL
SFP1_TX_DISABLE
SFP1_MODDEF
SFP1_RS1
SFP0_SCL
SFP2_RS0
PL_UART_TXD
SFP0_MODDEF
SFP2_SDA
SFP2_MODDEF
SFP1_TX_FAULT
SFP1_RS0
SFP2_RS1
SFP3_SDA
SFP1_RX_LOS
SFP2_TX_DISABLE
SFP2_RX_LOS
SFP3_TX_DISABLE
SFP2_TX_FAULT
SFP2_SCL
SFP3_SCL
SFP3_TX_FAULT
SFP3_MODDEF
SFP0_RS1
SFP3_RX_LOS
SFP3_RS0
LM75_SDA
PCIE_RESET
USER_LED_3
SFP3_RS1
SFP0_RS0
SFP0_RX_LOS
USER_LED_2
USER_LED_1
IIC_SCL
IIC_SDA
USER_LED_0
USER_PB_RESET
USER_PB_2
USER_PB_1
USER_PB_0
LM75_SCL
DDR3_SCL
DDR3_SDA
LM75_OS

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pcie reset
复位

按键

Title MC01,Bank 17, 18

Size: A4

Number:

Revision:A

Date:

Time:

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File:

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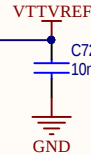
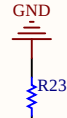
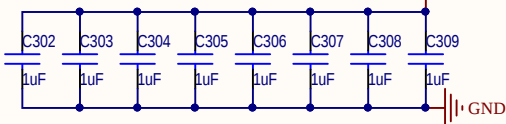
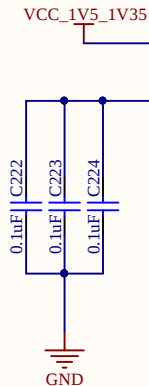


U1I

BANK32

IO_25_VRP_32	AB14	DNP
IO_L24N_T3_32	Y15	DDR3_DQ7
IO_L24P_T3_32	Y16	DDR3_DM0
IO_L23N_T3_32	AA16	DDR3_DQ1
IO_L23P_T3_32	AA17	DDR3_DQ4
IO_L22N_T3_32	AD14	DDR3_DQ3
IO_L22P_T3_32	AC14	DDR3_DQ2
IO_L21N_T3_DQS_32	AC15	DDR3_DQS0_N
IO_L21P_T3_DQS_32	AC16	DDR3_DQS0_P
IO_L20N_T3_32	AB15	DDR3_DQ5
IO_L20P_T3_32	AA15	DDR3_DQ0
IO_L19N_T3_VREF_32	AE14	VTTVREF
IO_L19P_T3_32	AE15	DDR3_DQ6
IO_L18N_T2_32	AC17	DDR3_DM1
IO_L18P_T2_32	AC19	DDR3_DQ10
IO_L17N_T2_32	AB19	DDR3_DQ8
IO_L17P_T2_32	AB18	DDR3_DQ13
IO_L16N_T2_32	AA18	DDR3_DQ12
IO_L16P_T2_32	Y18	DDR3_DQS1_N
IO_L15N_T2_DQS_32	Y19	DDR3_DQS1_P
IO_L15P_T2_DQS_32	AD16	DDR3_DQ9
IO_L14N_T2_SRCC_32	AD17	DDR3_DQ11
IO_L14P_T2_SRCC_32	AE18	DDR3_DQ14
IO_L13N_T2_MRCC_32	AD18	DDR3_DQ15
IO_L13P_T2_MRCC_32	AG17	DDR3_DM2
IO_L12N_T1_MRCC_32	AG18	DDR3_DQ18
IO_L12P_T1_MRCC_32	AF18	DDR3_DQ19
IO_L11N_T1_SRCC_32	AE19	DDR3_DQ22
IO_L11P_T1_SRCC_32	AD19	DDR3_DQ23
IO_L10N_T1_32	AK18	DDR3_DQS2_N
IO_L10P_T1_32	AJ18	DDR3_DQS2_P
IO_L9N_T1_DQS_32	AH19	DDR3_DQ20
IO_L9P_T1_DQS_32	AG19	DDR3_DQ16
IO_L8N_T1_32	AK19	DDR3_DQ17
IO_L8P_T1_32	AJ19	DDR3_DQ21
IO_L7N_T1_32	AF16	VTTVREF
IO_L7P_T1_32	AE16	DDR3_DM3
IO_L6N_T0_VREF_32	AJ17	DDR3_DQ25
IO_L6P_T0_32	AH17	DDR3_DQ28
IO_L5N_T0_32	AG14	DDR3_DQ29
IO_L5P_T0_32	AF15	DDR3_DQ27
IO_L4N_T0_32	AJ16	DDR3_DQS2_N
IO_L4P_T0_32	AH16	DDR3_DQS2_P
IO_L3N_T0_DQS_32	AH15	DDR3_DQ30
IO_L3P_T0_DQS_32	AG15	DDR3_DQ33
IO_L2N_T0_32	AK15	DDR3_DQ31
IO_L2P_T0_32	AK16	DDR3_DQ24
IO_L1N_T0_32	Y14	
IO_L1P_T0_32		
IO_0_VRN_32		

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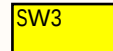
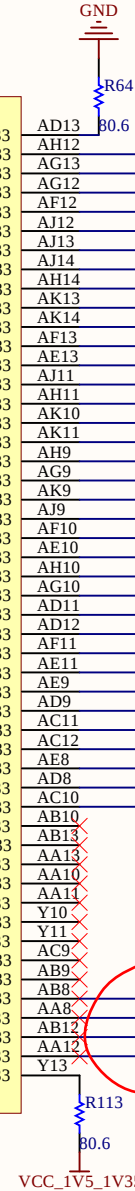
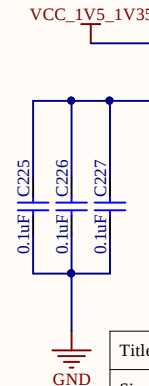


U1J

BANK33

IO_25_VRP_33	AD13	B0.6
IO_L24N_T3_33	AH12	DDR3_A0
IO_L24P_T3_33	AG13	DDR3_A1
IO_L23N_T3_33	AG12	DDR3_A2
IO_L23P_T3_33	AF12	DDR3_A3
IO_L22N_T3_33	AJ12	DDR3_A4
IO_L22P_T3_33	AJ13	DDR3_A5
IO_L21N_T3_DQS_33	AJ14	DDR3_A6
IO_L21P_T3_DQS_33	AH14	DDR3_A7
IO_L20N_T3_33	AK13	DDR3_A8
IO_L20P_T3_33	AK14	DDR3_A9
IO_L19N_T3_VREF_33	AF13	DDR3_A10
IO_L19P_T3_33	AE13	DDR3_A11
IO_L18N_T2_33	AJ11	DDR3_A12
IO_L18P_T2_33	AH11	DDR3_A13
IO_L17N_T2_33	AK10	DDR3_A14
IO_L17P_T2_33	AK11	DDR3_A15
IO_L16N_T2_33	AH9	DDR3_BA0
IO_L16P_T2_33	AG9	DDR3_BA1
IO_L15N_T2_DQS_33	AK9	DDR3_BA2
IO_L15P_T2_DQS_33	AJ9	DDR3_TEMP_EVENT
IO_L14N_T2_SRCC_33	AF10	DDR3_CKE0
IO_L14P_T2_SRCC_33	AE10	DDR3_CKE1
IO_L13N_T2_MRCC_33	AH10	DDR3_CK0_N
IO_L13P_T2_MRCC_33	AG10	DDR3_CK0_P
IO_L12N_T1_MRCC_33	AD11	SYSCLK_N
IO_L12P_T1_MRCC_33	AD12	SYSCLK_P
IO_L11N_T1_SRCC_33	AF11	DDR3_CK1_N
IO_L11P_T1_SRCC_33	AE11	DDR3_CK1_P
IO_L10N_T1_33	AE9	DDR3_WE_N
IO_L10P_T1_33	AD9	DDR3_RAS_N
IO_L9N_T1_DQS_33	AC11	DDR3_CAS_N
IO_L9P_T1_DQS_33	AC12	DDR3_S0_N
IO_L8N_T1_33	AE8	DDR3_S1_N
IO_L8P_T1_33	AD8	DDR3_ODT0
IO_L7N_T1_33	AC10	DDR3_ODT1
IO_L7P_T1_33	AB10	
IO_L6N_T0_VREF_33	AB13	
IO_L6P_T0_33	AA13	
IO_L5N_T0_33	AA10	
IO_L5P_T0_33	AA11	
IO_L4N_T0_33	Y10	
IO_L4P_T0_33	Y11	
IO_L3N_T0_DQS_33	AC9	
IO_L3P_T0_DQS_33	AB9	
IO_L2N_T0_33	AB8	USER_SW_0
IO_L2P_T0_33	AA8	USER_SW_1
IO_L1N_T0_33	AB12	USER_SW_2
IO_L1P_T0_33	AA12	USER_SW_3
IO_0_VRN_33	Y13	

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Title MC01,Bank 32, 33

Size: A4

Number:

Revision:A

Date:

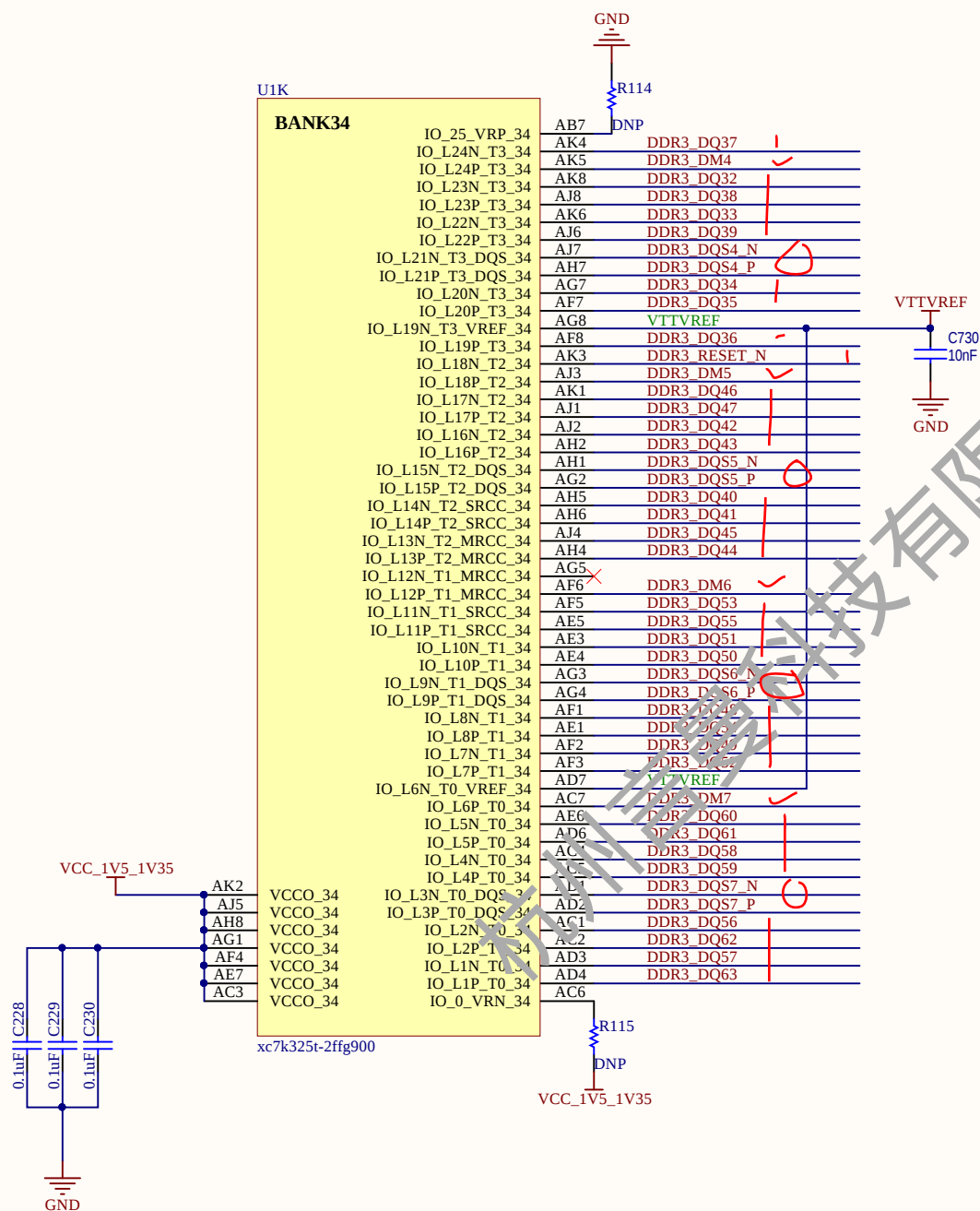
Time:

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File:

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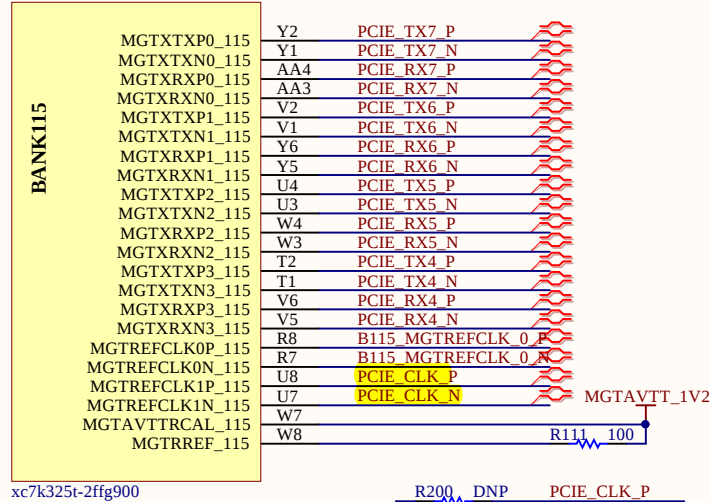




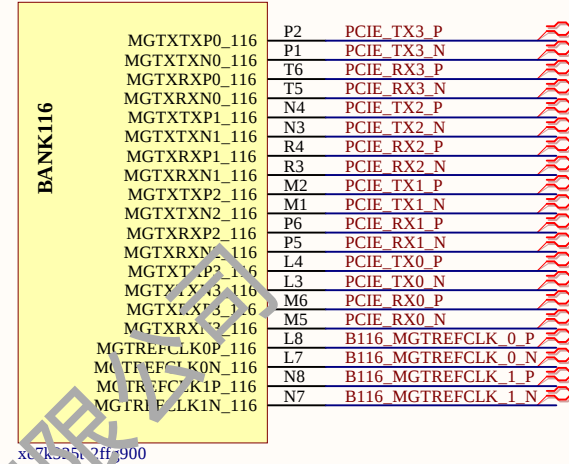
Title <i>MC01,Bank 34</i>			Hangzhou Yanman Co. Ltd. 杭州言曼科技有限公司 www.gvi-tech.com	
Size: A4	Number:	Revision: A		
Date:	Time:	Sheet 7 of 23		
File:				



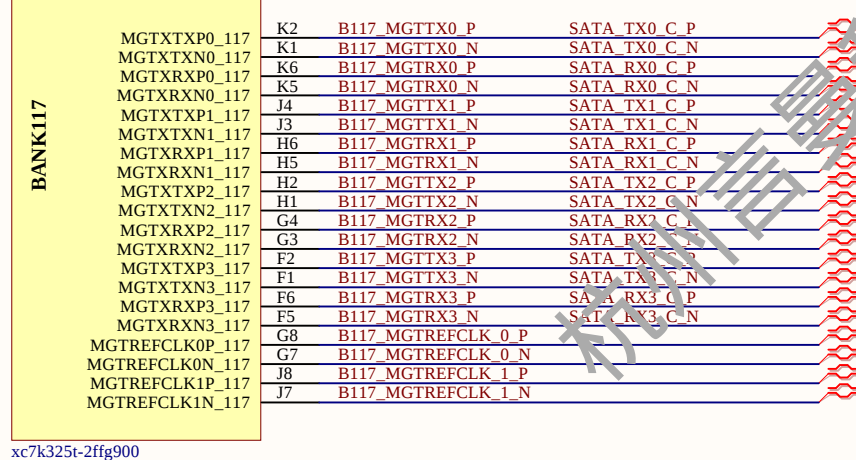
U1L



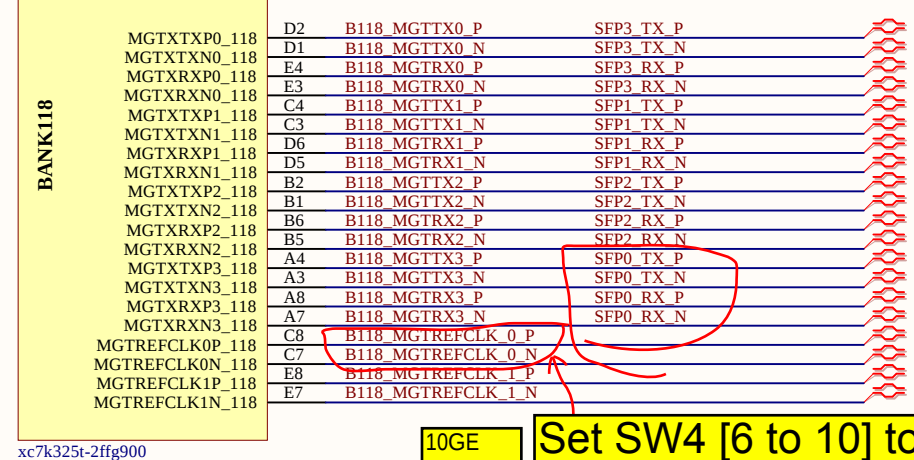
U1M



U1N



U1O



10GE

Set SW4 [6 to 10] to ON-OFF-OFF-OFF-ON.
This sets the frequency of U4 output to 156.25MHz.

Title **MC01,Bank GT**Size: **A4**

Number:

Revision:**A**

Date:

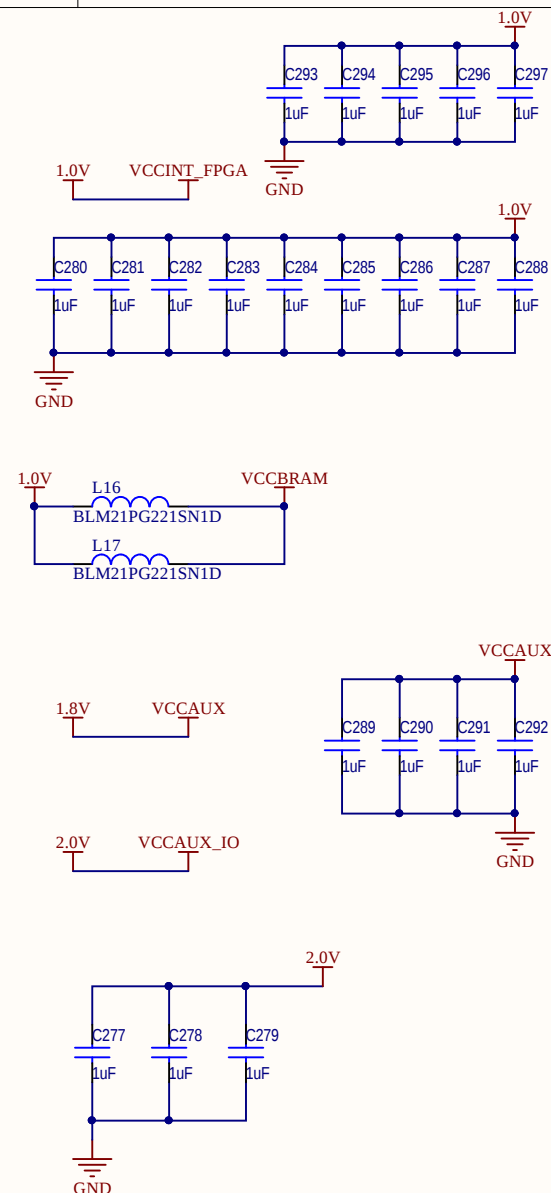
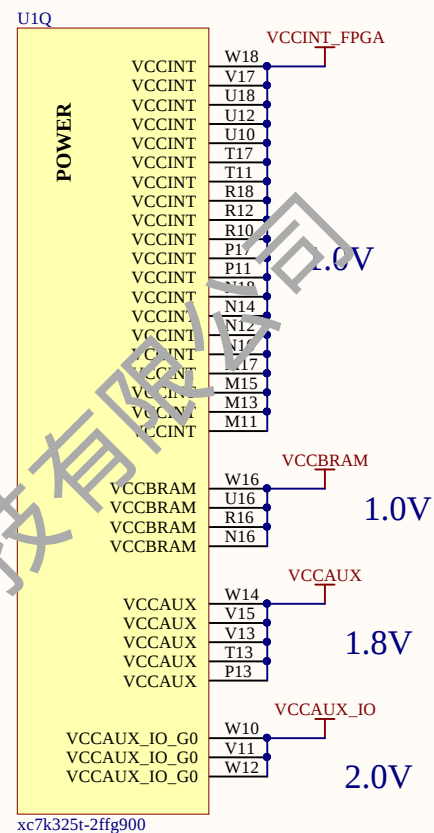
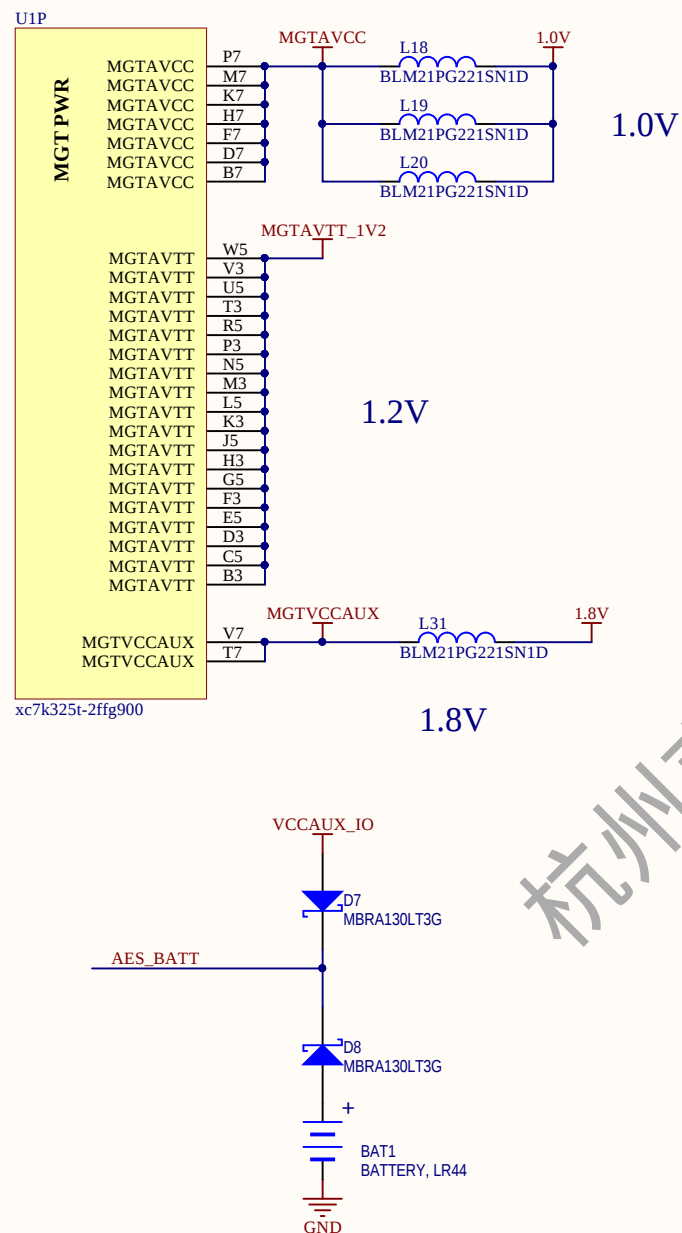
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File:

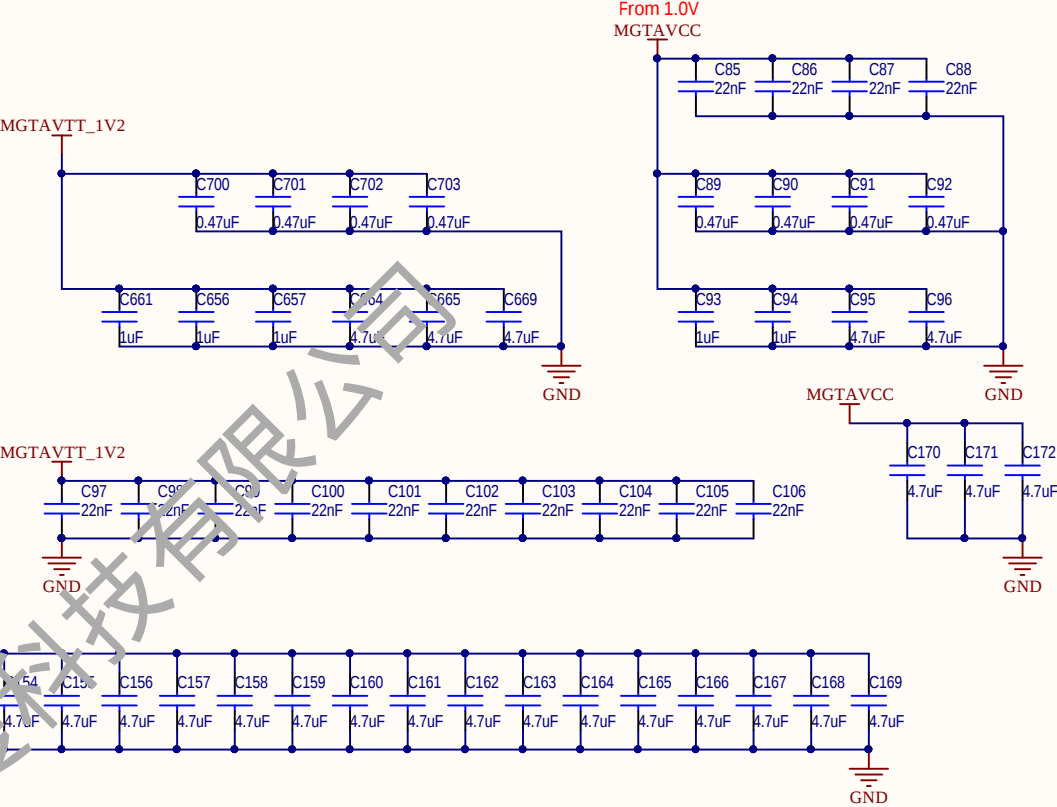
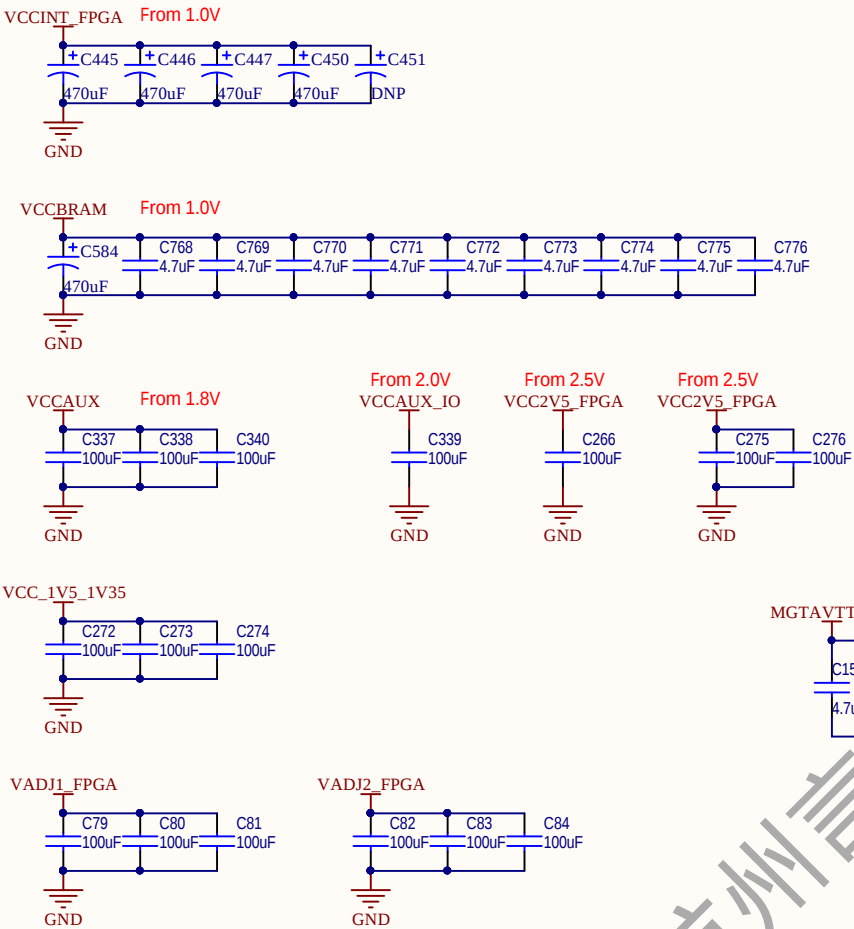
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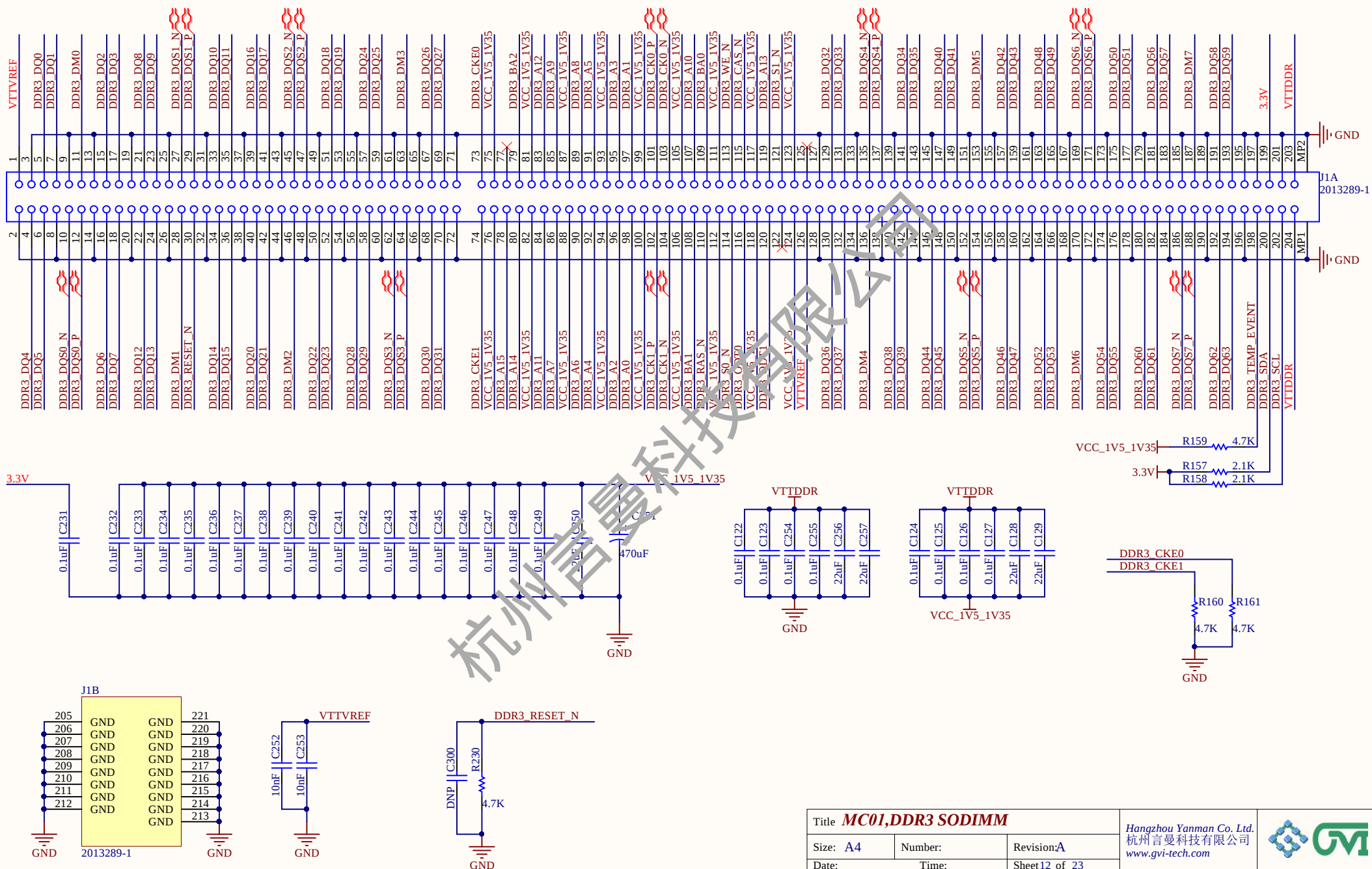




Title <i>MC01,FPGA Power</i>			Hangzhou Yanman Co. Ltd. 杭州言曼科技有限公司 www.gvi-tech.com 
Size: A4	Number:	Revision: A	
Date:	Time:	Sheet 9 of 23	
File:			



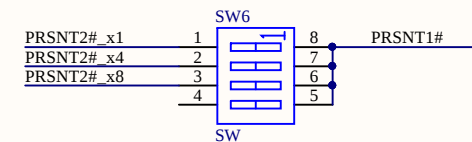
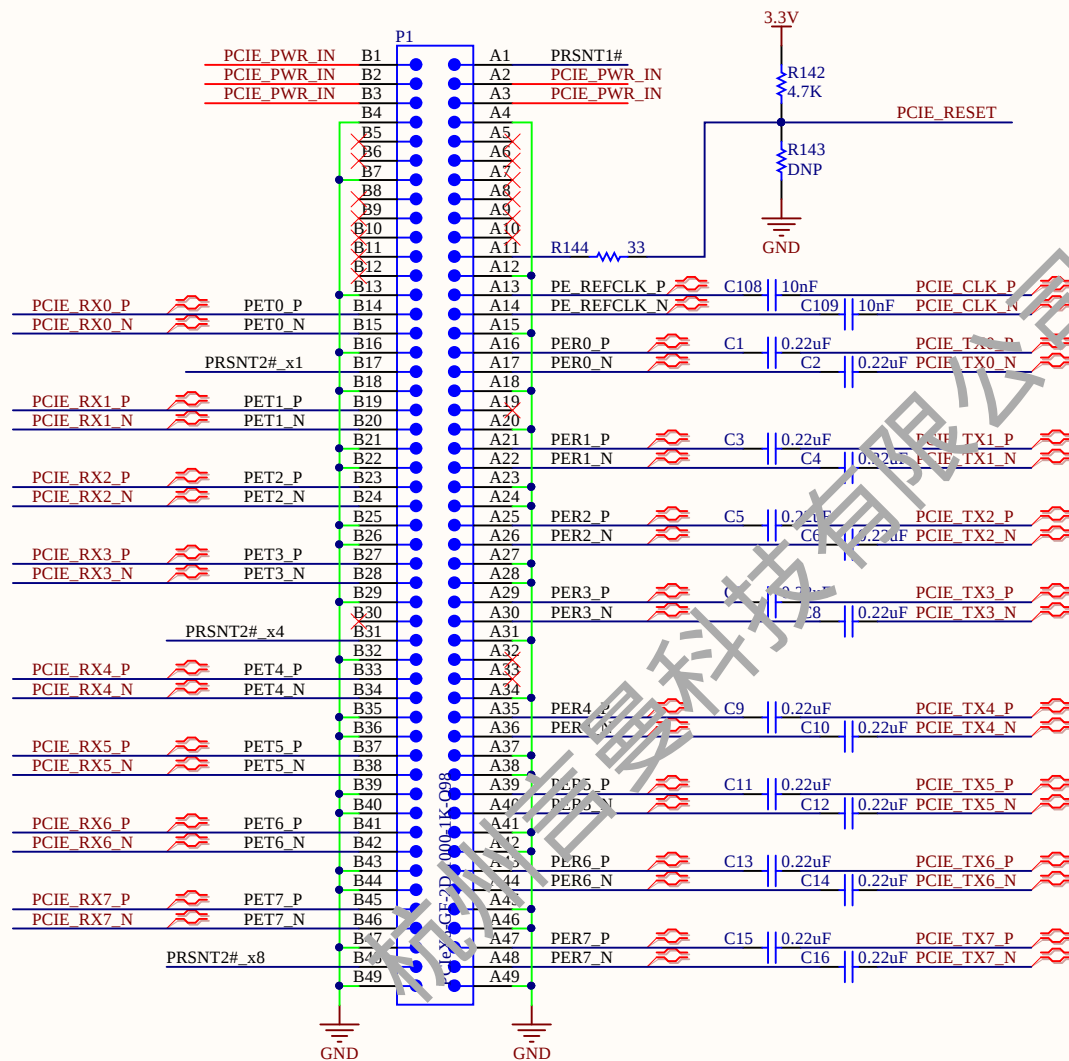


Title **MC01,DDR3 SODIMM**

Size: A4	Number:	Revision: A
Date:	Time:	Sheet 12 of 23
File:		

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Title **MC01, PCIe Gen2 X8**Size: **A4**

Number:

Revision: **A**

Date:

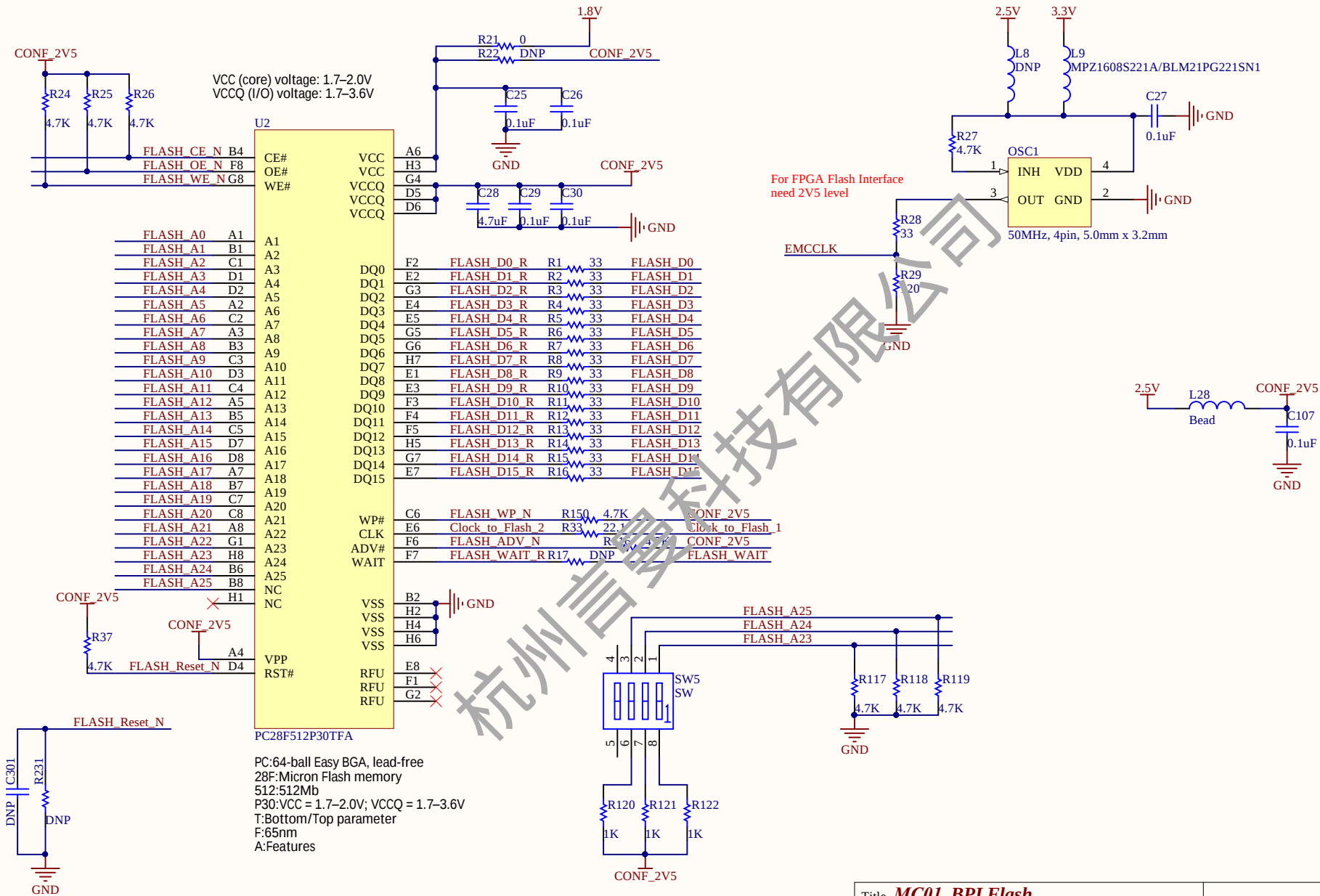
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File:

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Title **MC01, BPI Flash**Size: **A4**

Number:

Revision: **A**

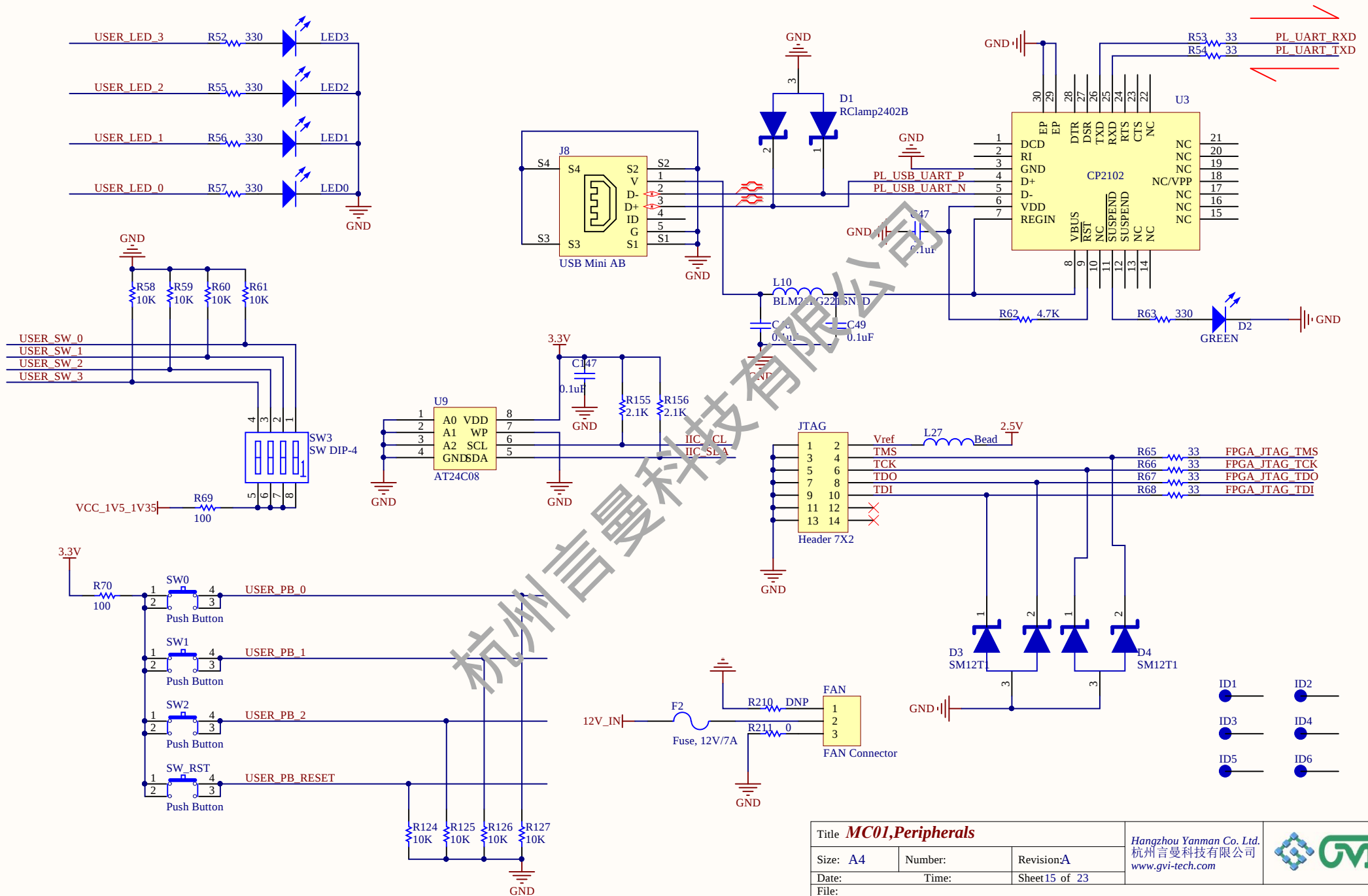
Date:

Time:

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File:

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Title **MC01,Peripherals**Size: **A4**

Number:

Revision: **A**

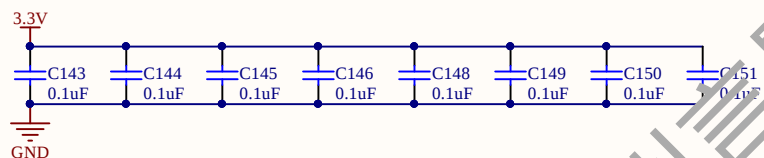
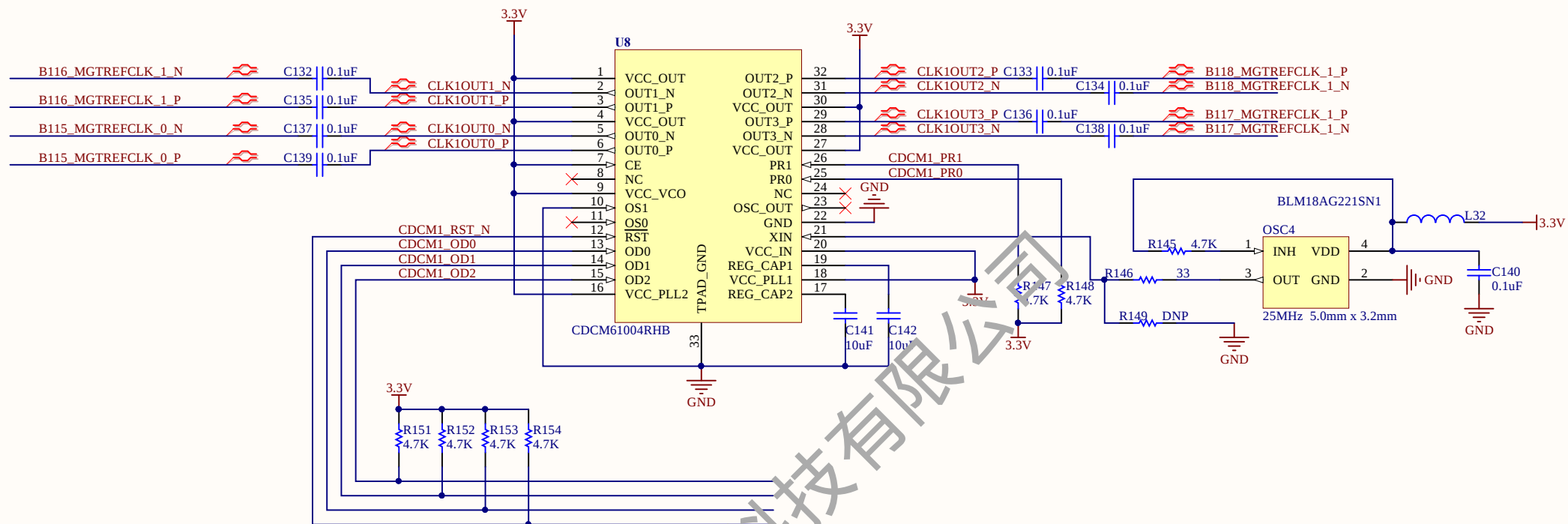
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File:

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单板上U8不焊接
不需要使用

SW1						Prescale	Feedback	PR1/PR0	VCO	Output	OD2/OD1	Output	Application
[1]	[2]	[3]	[4]	[5]	[6]	Divider	Divider		MHz	Divider	/OD0	MHz	
OFF	OFF	OFF	OFF	OFF	X	4	20	11	2000	8	111	62.5	GigE
OFF	OFF	OFF	ON	ON	X	3	24	00	1800	8	111	75	SATA
OFF	ON	OFF	ON	ON	X	3	24	00	1800	6	101	100	PCIE
OFF	OFF	ON	OFF	OFF	X	4	20	11	2000	4	011	125	GigE
OFF	OFF	ON	ON	ON	X	3	24	00	1800	4	011	150	SATA
OFF	OFF	ON	OFF	ON	X	3	25	10	1875	4	011	156.25	10 GigE
OFF	ON	ON	ON	OFF	X	5	15	01	1875	2	001	187.5	12 GigE
ON	OFF	ON	ON	ON	X	3	24	00	1800	3	010	200	PCIE
OFF	ON	ON	OFF	OFF	X	4	20	11	2000	2	001	250	GigE
OFF	ON	ON	OFF	ON	X	3	25	10	1875	2	001	312.5	XGMII
ON	ON	ON	OFF	ON	X	3	25	10	1875	1	000	625	10 GigE

Title **MC01,Clock Generator**Size: **A4**

Number:

Revision:**A**

Date:

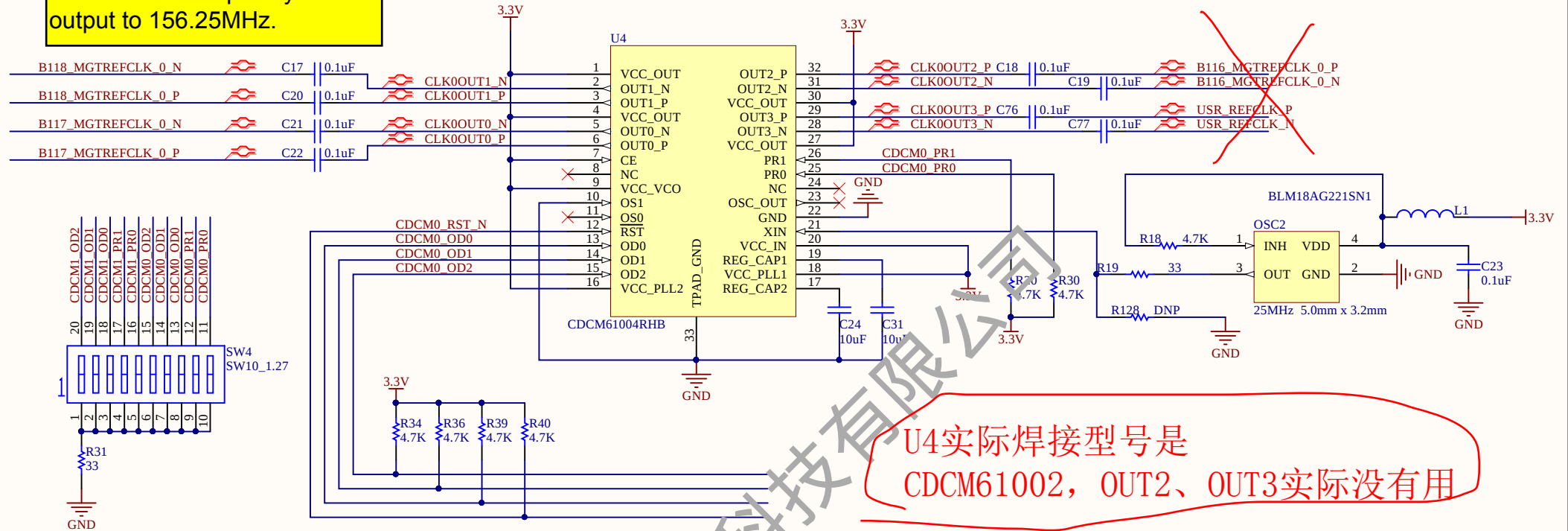
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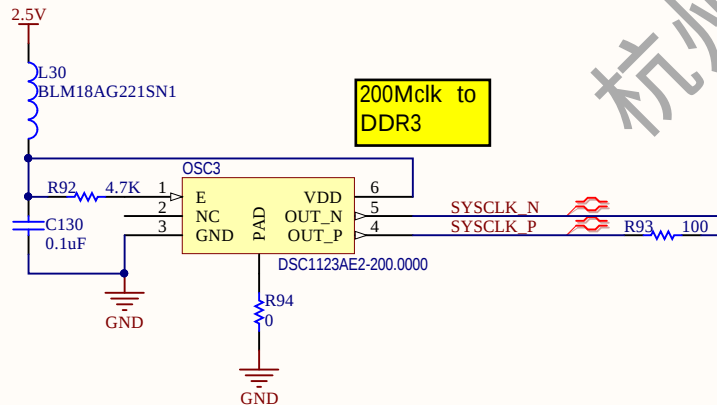
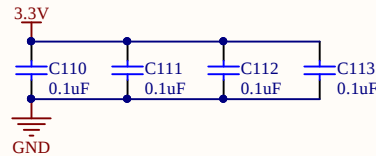
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Set SW4 [6 to 10] to ON-OFF-OFF-OFF-ON.
This sets the frequency of U4 output to 156.25MHz.



U4实际焊接型号是
CDCM61002, OUT2、OUT3实际没有用



SW1						Prescale	Feedback	PR1/PR0	VCO	Output	OD2/OD1	Output	Application
[1]	[2]	[3]	[4]	[5]	[6]	Divider	Divider		MHz	Divider	/OD0	MHz	
OFF	OFF	OFF	OFF	OFF	X	4	20	11	2000	8	111	62.5	GigE
OFF	OFF	OFF	ON	ON	X	3	24	00	1800	8	111	75	SATA
OFF	ON	OFF	ON	ON	X	3	24	00	1800	6	101	100	PCIE
OFF	OFF	ON	OFF	OFF	X	4	20	11	2000	4	011	125	GigE
OFF	OFF	ON	ON	ON	X	3	24	00	1800	4	011	150	SATA
OFF	OFF	ON	OFF	ON	X	3	25	10	1875	4	011	156.25	10 GigE
OFF	ON	ON	ON	OFF	X	5	15	01	1875	2	001	187.5	12 GigE
ON	OFF	ON	ON	ON	X	3	24	00	1800	3	010	200	PCIE
OFF	ON	ON	OFF	OFF	X	4	20	11	2000	2	001	250	GigE
OFF	ON	ON	OFF	ON	X	3	25	10	1875	2	001	312.5	XGMII
ON	ON	ON	OFF	ON	X	3	25	10	1875	1	000	625	10 GigE

Title **MC01, Clock Generator**

Size: **A4**

Number:

Revision: **A**

Date:

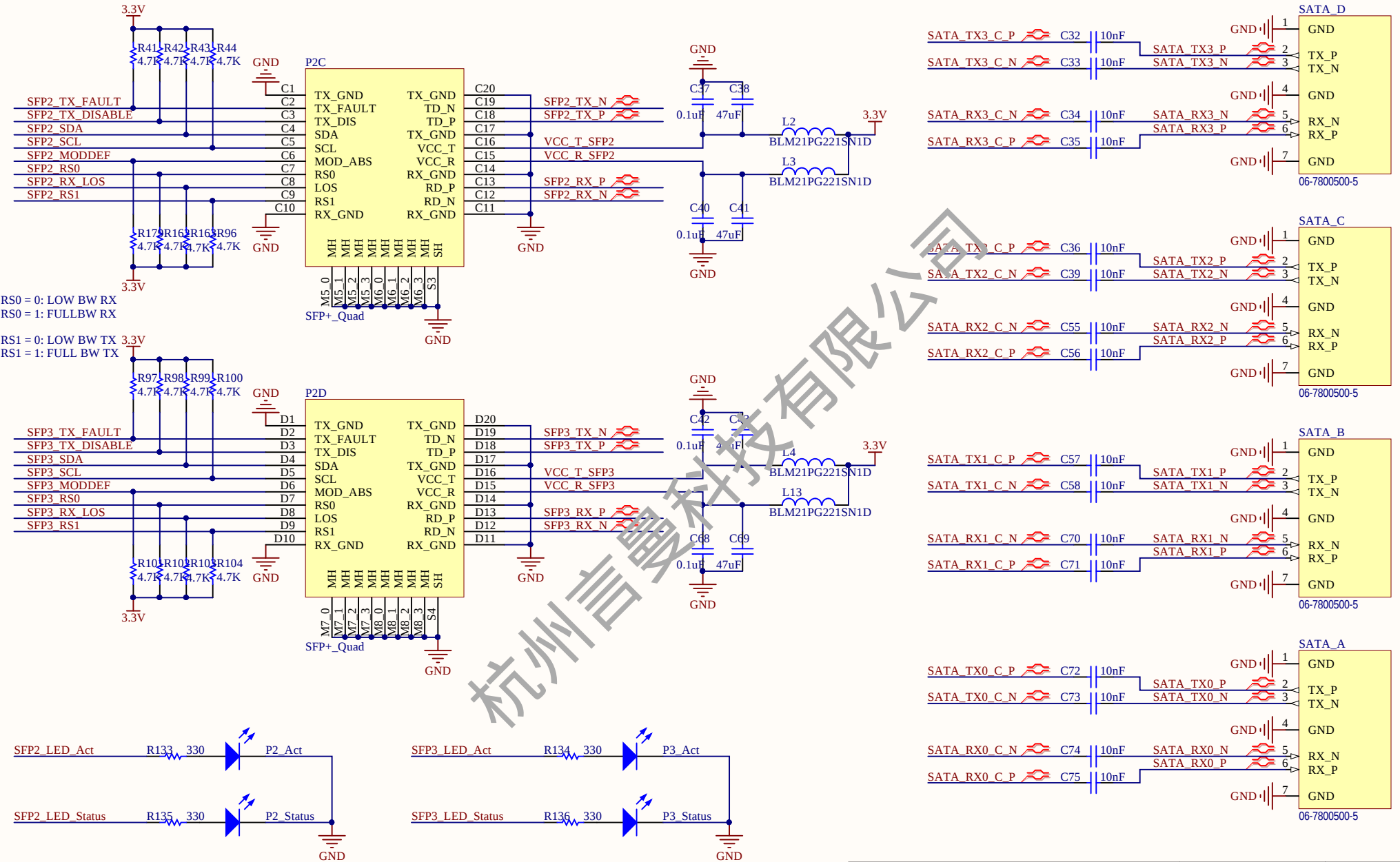
Time:

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File:

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Title **MC01,SFP+, SATA**Size: **A4**

Number:

Revision:**A**

Date:

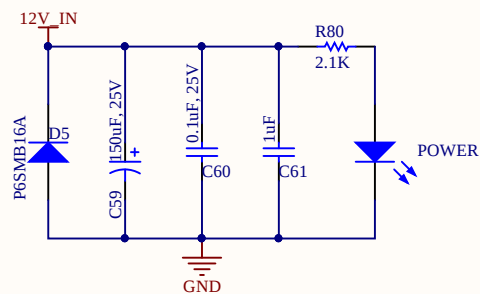
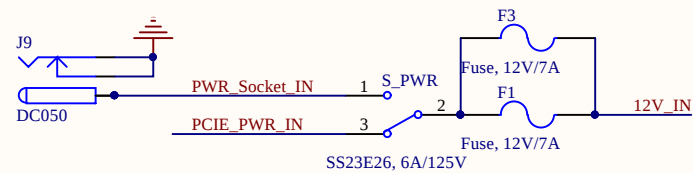
Time:

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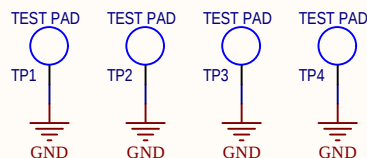
File:

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Title <i>MC01, SFP+</i>			Hangzhou Yanman Co. Ltd. 杭州言曼科技有限公司 www.gvi-tech.com	
Size: A4	Number:	Revision: A		
Date:	Time:	Sheet 18 of 23		
File:				



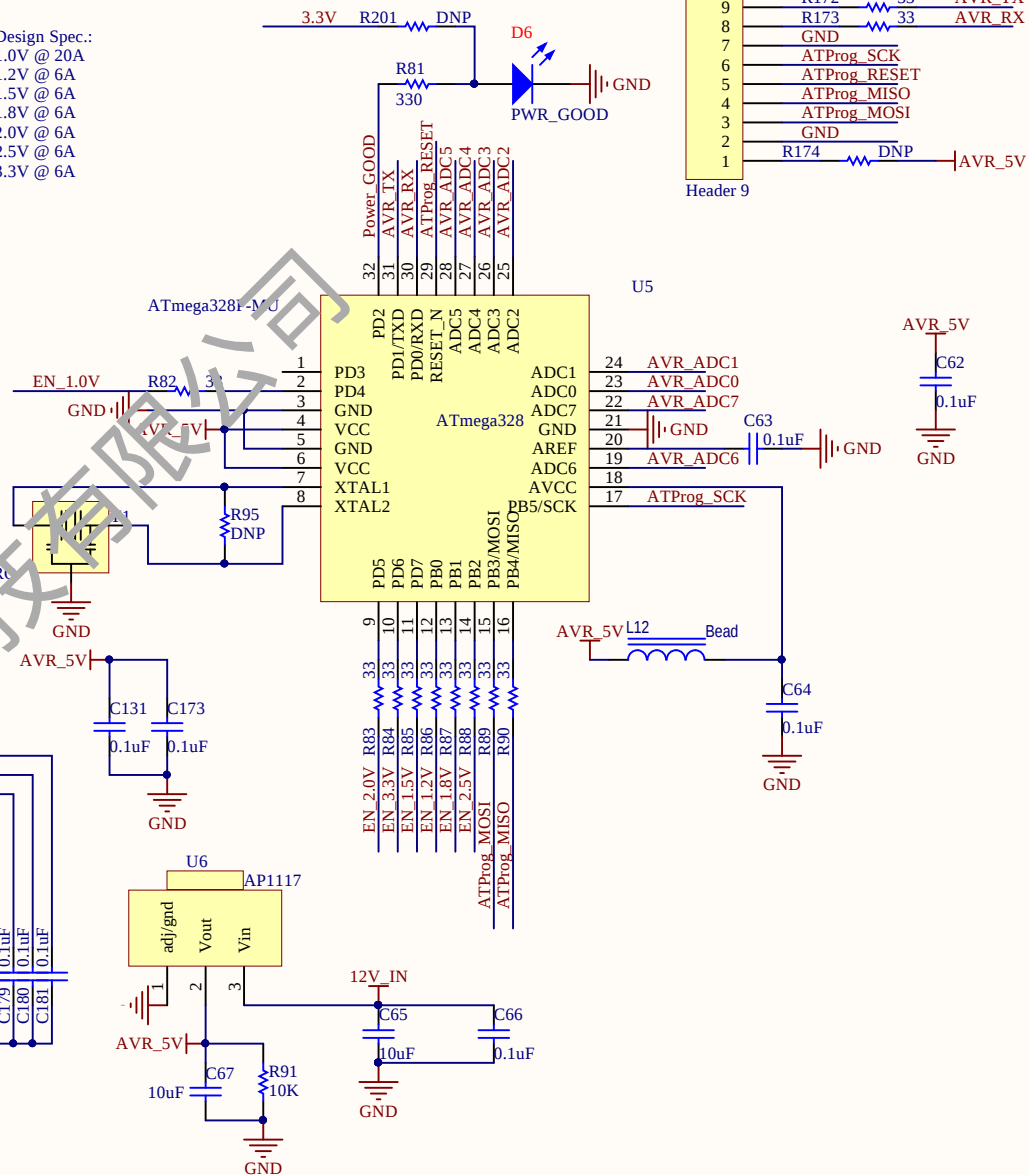
1.0V->"MGTA VCC","VCCINT_FPGA","VCCBRAM"
MGTA VTT_1V2
1.8V->"VCCAUX"
VCC_1V5_1V35
2.5V->"VCC2V5_FPGA","CONF_2V5"
2.0V->"VCCAUX_IO"
3.3V
VTTDDR
VTTVREF



Power-On Sequence:
1.0V --> 1.8V --> 1.5V & 2.0V --> 2.5V & 3.3V --> 1.2V

Design Spec.:
1.0V @ 20A
1.2V @ 6A
1.5V @ 6A
1.8V @ 6A
2.0V @ 6A
2.5V @ 6A
3.3V @ 6A

CSTCE16M0V52 R



Title **MC01,Power Management**

Size: **A4**

Number:

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Rrf (kΩ)	To	Rrf(KHz)
0	GND	250
187	GND	300
619	GND	400
OPEN	N/A	500
866	VREG	650
309	VREG	750
124	VREG	850
0	VREG	970

EN:max 7V

SOFT-START TIME:2.8ms

EN:min 1.6V;max 5V

1V2

$$V_{out}=0.765*(1+R1/R2)$$
$$V_{out}=0.765*(1+2.49/22)$$
$$V_{out}=1.20V$$

1V8

$$V_{out}=0.765*(1+R1/R2)$$
$$V_{out}=0.765*(1+32/22.1)$$
$$V_{out}=1.87V$$

Title **MC01, Power Supplier**Size: **A4**

Number:

Revision:**A**

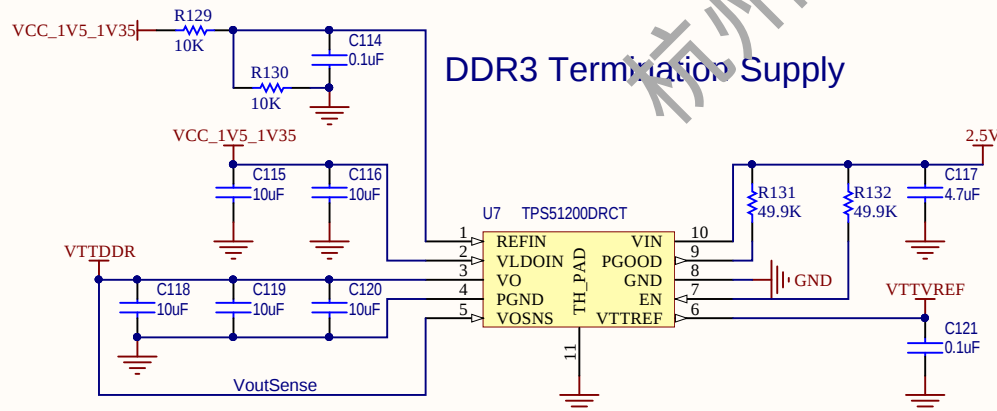
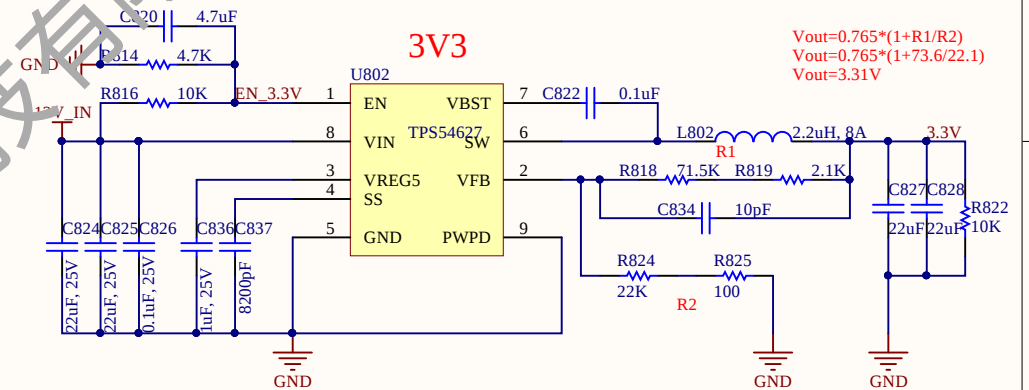
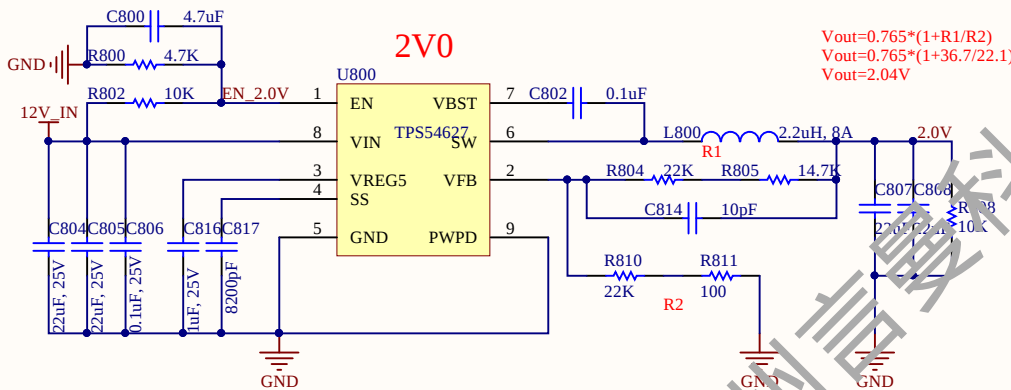
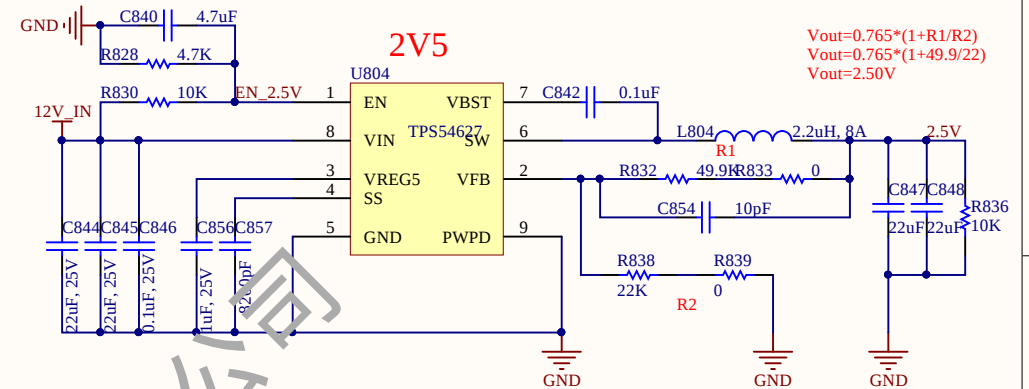
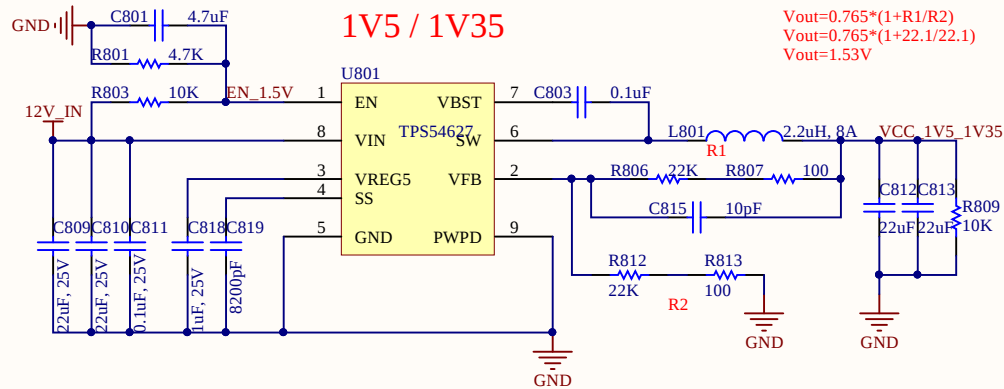
Date:

Time:

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File:

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Title **MC01,Power Supplier**

Size: **A4**

Number:

Revision:**A**

Date:

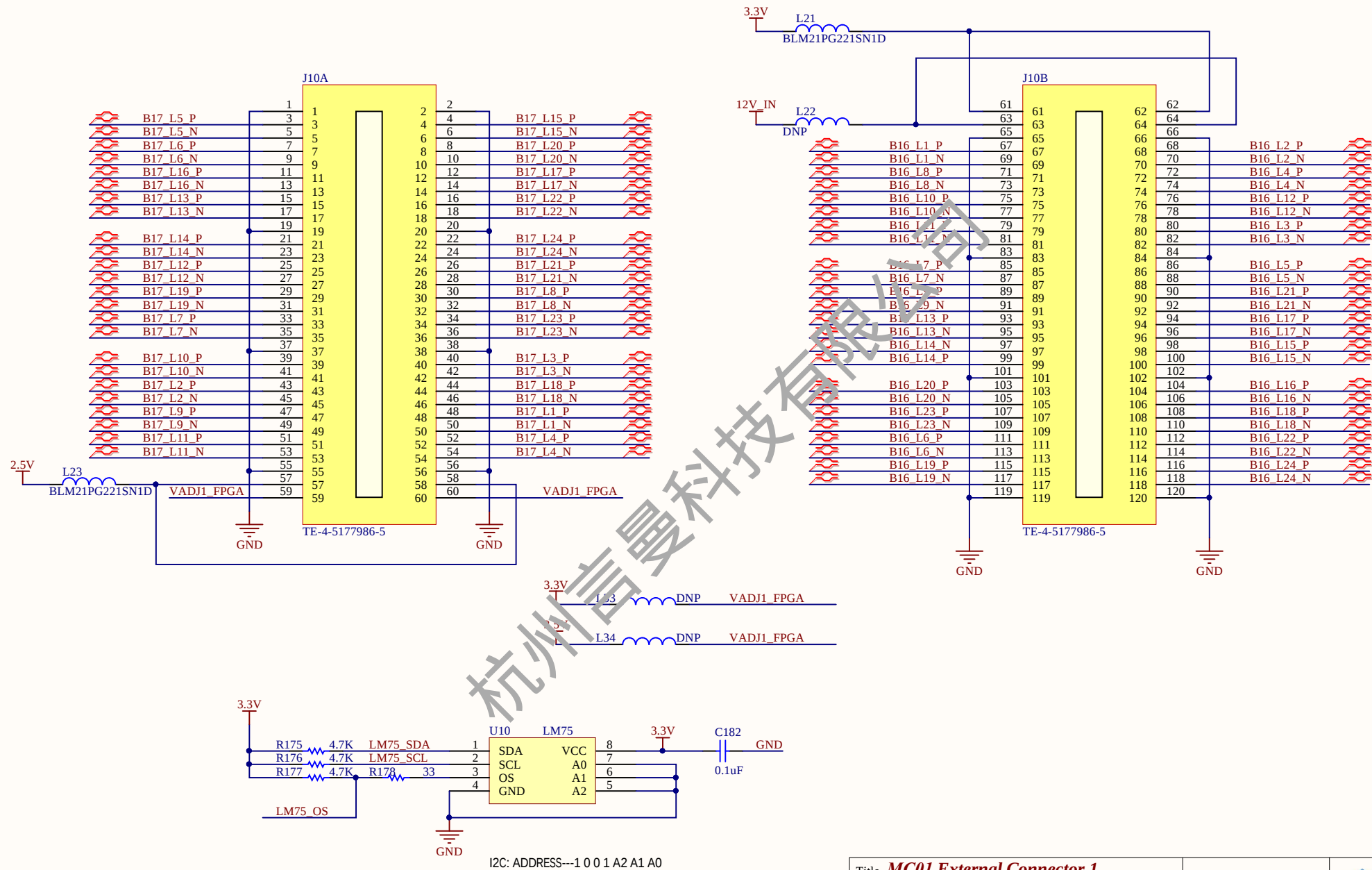
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Title **MC01,External Connector 1**Size: **A4**

Number:

Revision:**A**

Date:

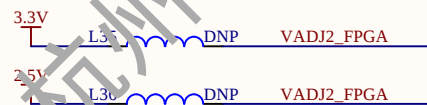
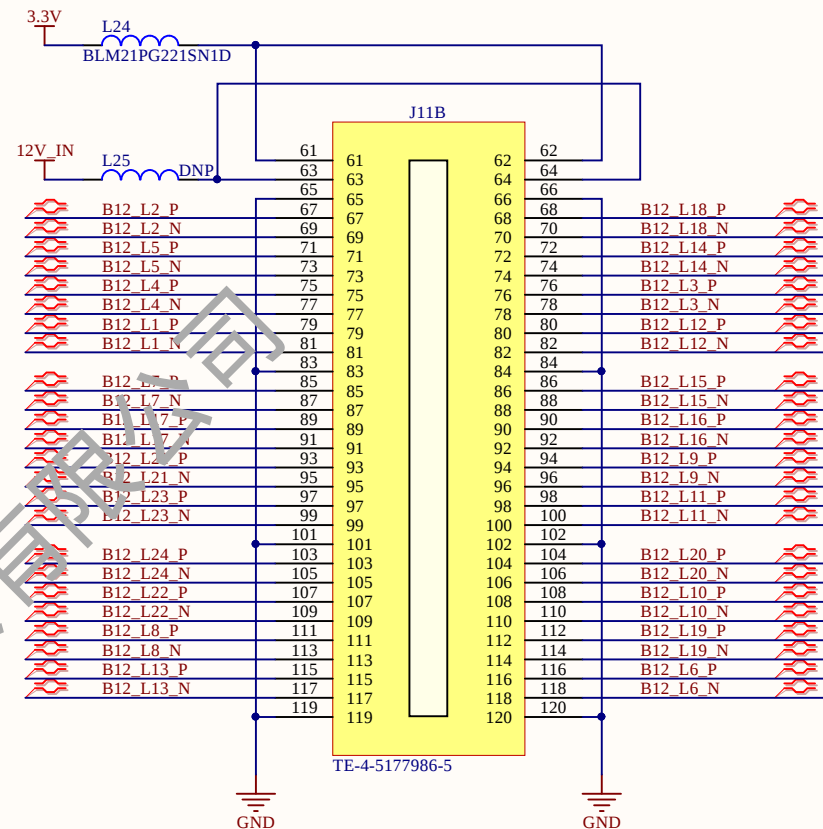
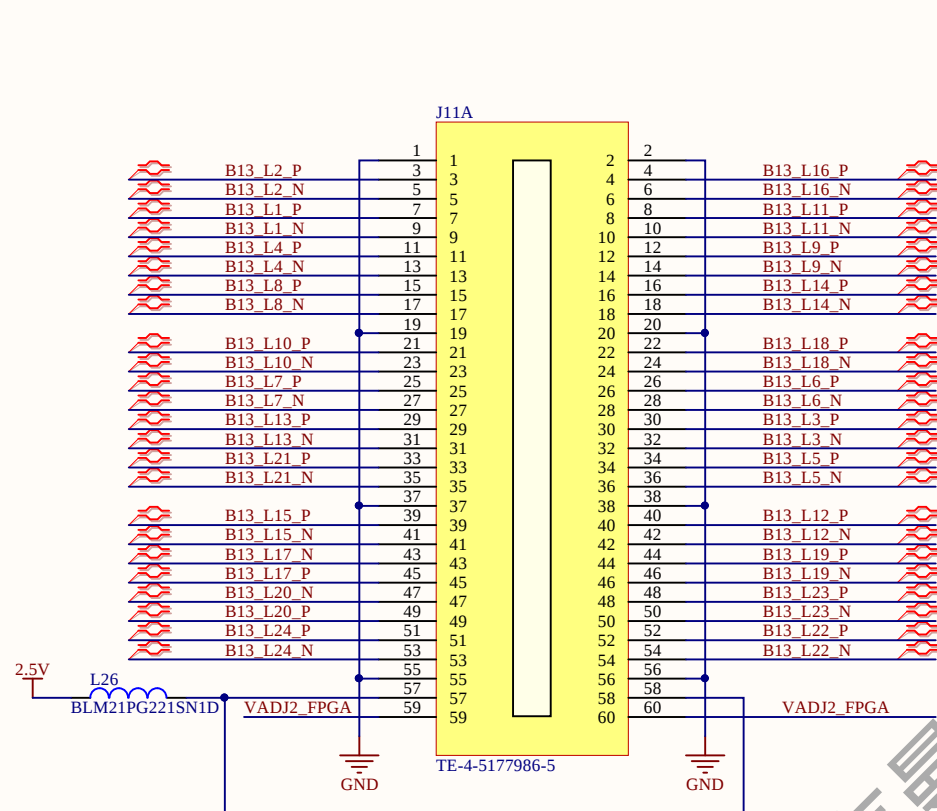
Time:

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Title **MC01,External Connector 2**Size: **A4**

Number:

Revision:**A**

Date:

Time:

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