



ALGOLTEK

AG9310

付S 18027661972 Q:1540182856

**Type C to HDMI
Converter**

Data Sheet

Official Version

V1.1

October, 2017

Revision History

Version	Date	Notes
1.0.0	2017/8/29	First release
1.0.1	2017/09/19	Modify MBQ pin description
1.0.2	2017/10/13	Modify pin description order.
1.1.0	2017/10/15	Template modification

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I. General Description

ALGOLTEK AG9310 is a single chip solution to implement USB Type-C to HDMI data converter. With USB Type-C DisplayPort Alternate Mode supporting, AG9310 can transmit both video and audio streams from USB Type-C interface to HDMI Port. In AG9310, DisplayPort v1.2 receiver can support different configurations by 1, 2 and 4 lanes @1.62Gbps, 2.7Gbps and 5.4Gbps frequency input, and HDMI supports 4K2K@30Hz output. Product manufactures can easily implement Type-C video conversion dongles and dockings by using AG9310 application.

II. Features

- Embedded 16 bit MCU
- EDID and MCCS pass-through supported
- Supports Hot Plug Detection
- External SPI flash supported for firmware upgrade
- Embedded HDCP 1.4 supported
- HDMI 1.4b TX supports 4K@30Hz output
- 1.2V Core power and 3.3V I/O power
- 2KV ESD performance
- Down Spread Spectrum Clock (SSC) supported

III. Device Information

Part Number	Package	Body Size	Note
AG9310-MBQ	QFN-48	6x6 mm ²	/wo I ² S audio output
AG9310-MCQ	QFN-64	8x8 mm ²	/w I ² S audio output

IV. Application

- USB Type-C dongle
- USB Type-C docking station
- TV/Projector Type-C interface

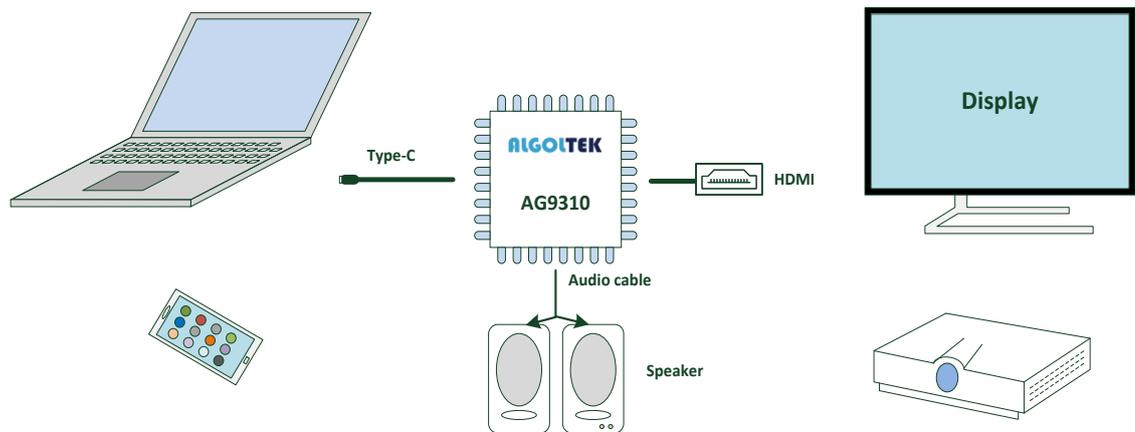


Figure 1 Application for Type-C to HDMI Dongle

V. System Block Diagram

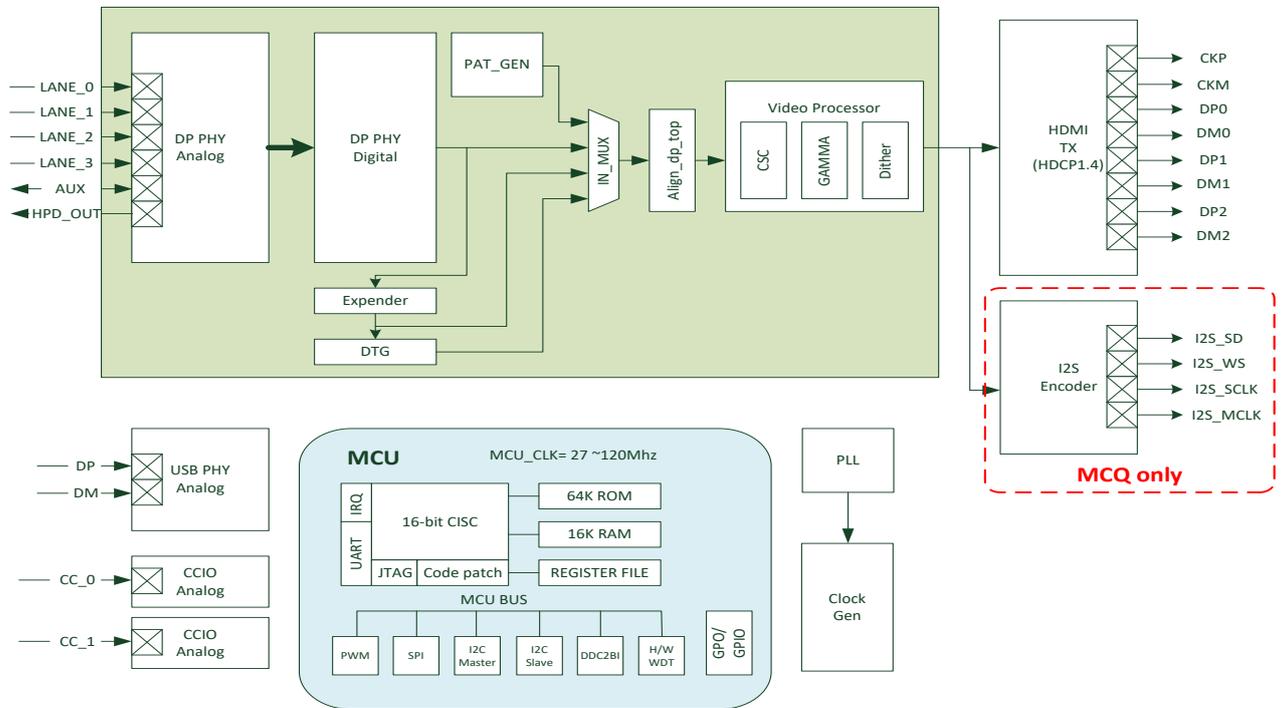


Figure 2 System Block Diagram

VI. Pin Mapping and Description

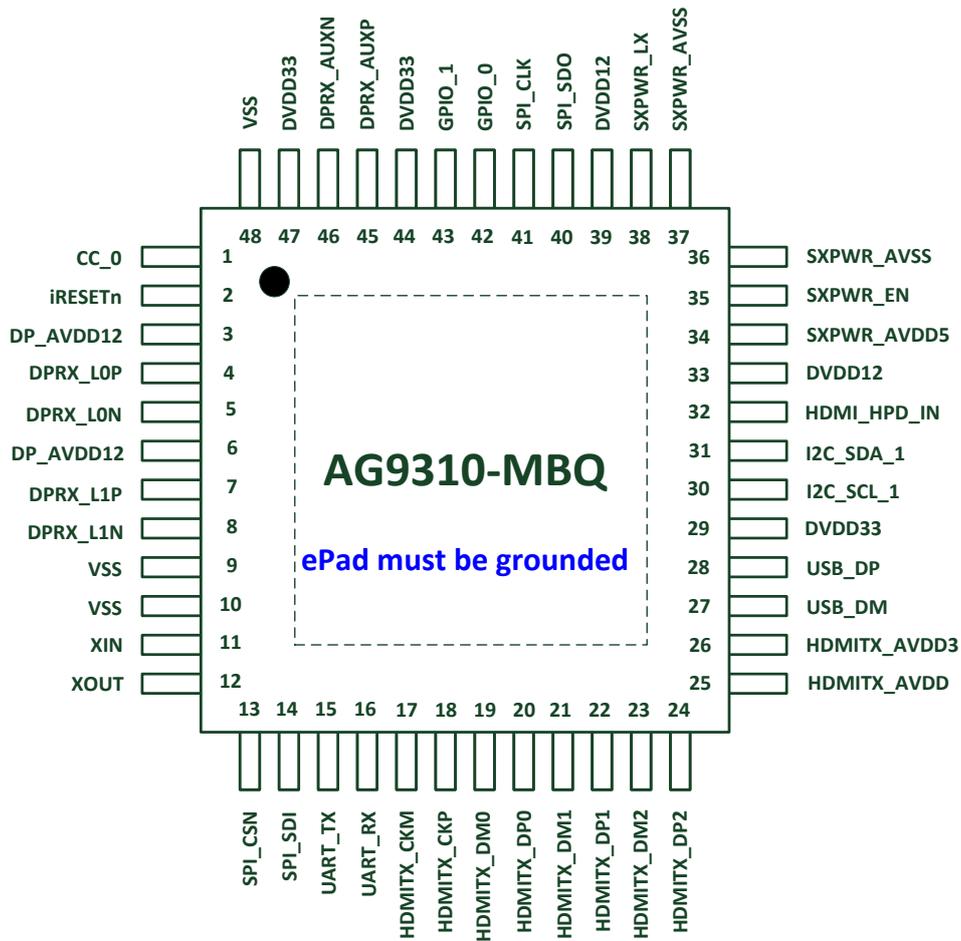


Figure 3 AG9310-MBQ PIN Mapping

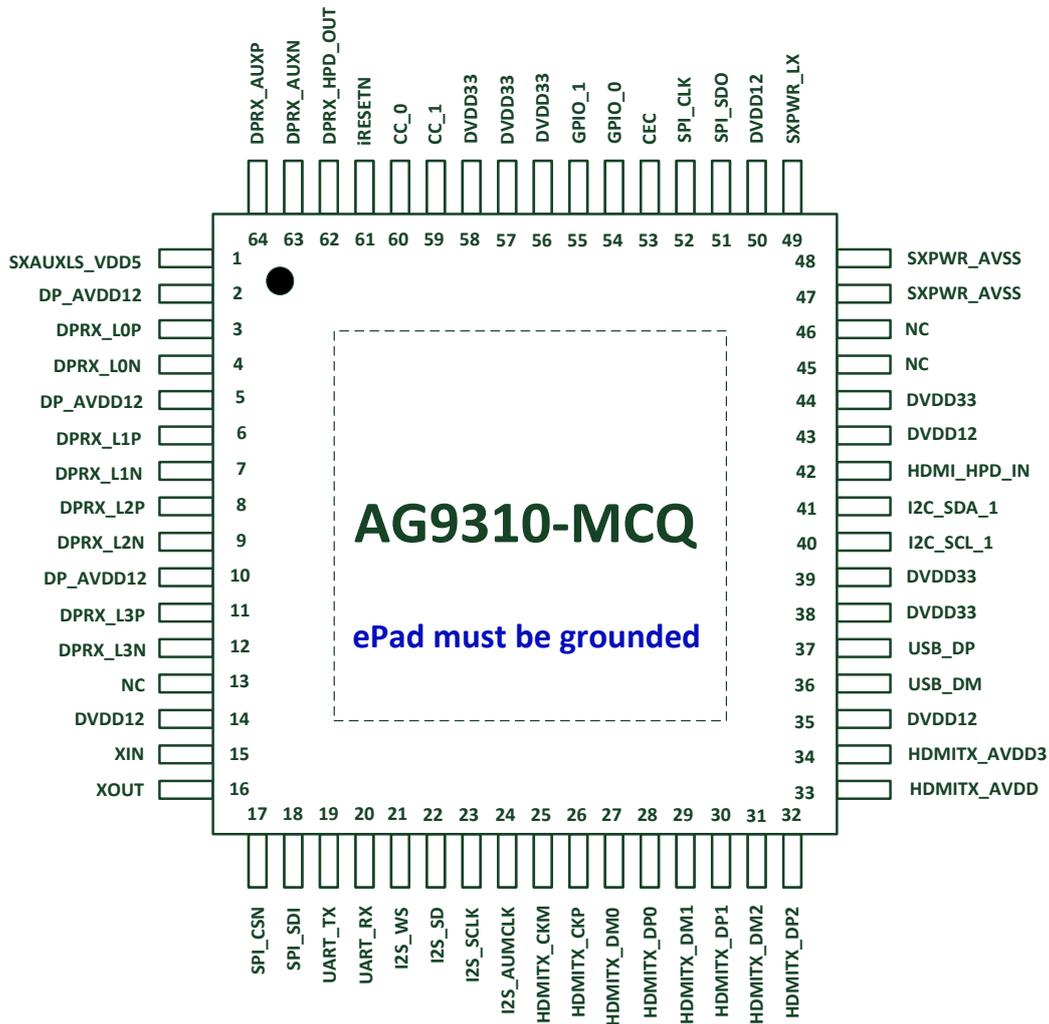


Figure 4 AG9310-MCQ PIN Mapping

Table 1 PIN Description

Pin Name	PIN NO.		Type	Description
	MBQ	MCQ		
POWER SUPPLY				
SXAUXLS_VDD5		1	Power	Analog 5V power input for AUX channel
DP_AVDD12	3,6	2, 5, 10	Power	Analog 1.2V power input for DP RX
DVDD33	29, 44, 47	38, 39, 44, 56, 57, 58	Power	Digital 3.3V I/O power input

DVDD12	33, 39	14, 35, 43, 50	Power	Digital 1.2V core power input
VSS	9, 10, 48		Power	Digital ground
HDMITX_AVDD	25	33	Power	Analog 1.2V power for HDMI TX
HDMITX_AVDD3	26	34	Power	Analog 3.3V power for HDMI TX
SXPWR_AVDD5	34		Power	5.0V power input. Input voltage range: 3.0V ~ 5.5V
SXPWR_AVSS	36, 37	47, 48	Power	Analog ground.
SXPWR_LX	38	49	Power	NC
DIFFERENTIAL HIGH-SPEED IO				
DPRX_LOP	4	3	Input	DP RX lane0 positive
DPRX_LON	5	4	Input	DP RX lane0 negative
DPRX_L1P	7	6	Input	DP RX lane1 positive
DPRX_L1N	8	7	Input	DP RX lane1 negative
DPRX_L2P	-	8	Input	DP RX lane2 positive
DPRX_L2N	-	9	Input	DP RX lane2 negative
DPRX_L3P	-	11	Input	DP RX lane3 positive
DPRX_L3N	-	12	Input	DP RX lane3 negative
HDMITX_CKM	17	25	Output	HDMI TX clock channel negative
HDMITX_CKP	18	26	Output	HDMI TX clock channel positive
HDMITX_DM0	19	27	Output	HDMI TX data channel 0 negative
HDMITX_DP0	20	28	Output	HDMI TX data channel 0 positive
HDMITX_DM1	21	29	Output	HDMI TX data channel 1 negative
HDMITX_DP1	22	30	Output	HDMI TX data channel 1 positive
HDMITX_DM2	23	31	Output	HDMI TX data channel 2 negative
HDMITX_DP2	24	32	Output	HDMI TX data channel 2 positive
USB_DM	27	36	Bidirectional	USB Type-C D-
USB_DP	28	37	Bidirectional	USB Type-C D+
DPRX_AUXN	46	63	Bidirectional	DisplayPort AUX channel N
DPRX_AUXP	45	64	Bidirectional	DisplayPort AUX channel P

Digital IO				
XIN	11	15	Input	Crystal oscillator clock input
XOUT	12	16	Output	Crystal oscillator clock output
SPI_CSN	13	17	Output	SPI chip select.
SPI_SDI	14	18	Input	SPI data input
UART_TX	15	19	Output	UART TX
UART_RX	16	20	Input	UART RX
I2S_WS	-	21	Output	I2S Left Right Clock
I2S_SD	-	22	Output	I2S Serial Audio Data Output
I2S_SCLK	-	23	Output	I2S Continuous Serial Clock
I2S_AUMCLK	-	24	Output	I2S System Clock
I2C_SCL_1	30	40	Bidirectional	HDMI I2C SCL
I2C_SDA_1	31	41	Bidirectional	HDMI I2C SDA
HDMI_HPD_IN	32	42	Input	HDMI cable detection
SXPWR_EN	35	-	Input	Pull down to ground
SPI_SDO	40	51	Output	SPI data output.
SPI_CLK	41	52	Output	SPI clock.
CEC	-	53	Input	HDMI CEC
GPIO_0	42	54	Bidirectional	General Purpose I/O
GPIO_1	43	55	Bidirectional	General Purpose I/O
CC_1	-	59	Input	Type-C configuration channel
CC_0	1	60	Input	Type-C configuration channel
iRESETN	2	61	Input	H/W Reset signal, active low. Need connect to Resistor and Capacitor on board.
DPRX_HPD_OUT	-	62	Output	DP RX Hot Plug Detect

VII. Specification

i. Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDD5	5V Power Input	-0.5	5.5	V
VDD33/AVDD33	3.3V supply voltage	-0.5	3.63	V
VDD/AVDD	1.2V supply voltage	-0.5	1.32	V

Table 2 Absolute Maximum Rating

ii. DC Characteristics/Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
VDD5	5V Power Input	4.5	5	5.5	V
VDD33	Digital I/O supply voltage	3	3.3	3.6	V
VDD	Digital core supply voltage	1.16	1.2		V
AVDD3	Analog I/O supply voltage	3	3.3	3.6	V
AVDD	Analog core supply voltage	1.16	1.2		V
I _{VDD33+AVDD3}	3.3V I/O Supply Current(4K2K/30Hz)		80		mA
I _{VDD+AVDD}	1.2V Core supply Current(4K2K/30Hz)		380		mA
V _{OH}	Output High Voltage	2.4			V
V _{OL}	Output Low Voltage			0.4	V
V _{IH}	Input High Voltage	2.0		5.5	V
V _{IL}	Input Low Voltage	-0.3		0.8	V
I _{LI}	Input leakage Cur.			±1	uA
T _A	Ambient Temperature	0		70	°C

Table 3 Digital I/O Specification

iii. AC Characteristics

DisplayPort Main Link AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UI_HBR2	Unit interval for HBR2(5.4-Gbps/lane)		185		ps
UI_HBR	Unit interval for HBR(2.7-Gbps/lane)		370		ps
UI_RBR	Unit interval for RBR(1.62-Gbps/lane)		617		ps
Down_Spread_Amp.	Link clock down-spreading	0		0.5	%
Down_Spread_Frequency	Link clock down-spreading frequency	30		33	kHz
T _{RX-MEDIAN-to-MAX-JITTER}	Max time between the jitter median and max. deviation from the median at Rx package pins for HBR (2.7-Gbps)			0.265	UI
T _{RX-MEDIAN-to-MAX-JITTER}	Max. time between the jitter median and max. deviation from the median at Rx package pins for RBR (1.62-Gbps)			0.39	UI
V _{RX-DC-CM}	RX DC Common Mode Voltage	0		2	V
I _{RX-SHORT}	RX Short Circuit Current Limit			50	mA

Table 4 DisplayPort Input Timing

DisplayPort AUX-CH AC Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
UIMAN	AUX (Manchester transaction) unit interval	0.4	0.5	0.6	us
Pre-charge Pulses	Number of pre-charge pulses	10		16	
T _{AUX-BUS-PEAK}	AUX CH bus park time	10			ns
T _{cycle-to-cycle jitter}	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI
V _{AUX-DIFFp-p RX}	AUX peak-to-peak voltage at a transmitting device when receiving	0.29		1.38	V
V _{AUX-DIFFp-p RX}	AUX peak-to-peak voltage at a receiving device when receiving	0.27		1.36	V
V _{AUX_TERM_R}	AUX CH termination DC resistance		100		Ω
V _{AUX_DC_CM}	AUX DC common mode voltage	0		2.0	V
V _{AUX_TURN_CM}	AUX turn around common mode voltage			0.3	V
I _{AUX_SHORT}	AUX short circuit current			90	mA
C _{AUX}	AUX AC coupling	75		200	nF

Table 5 DisplayPort AUX Channel I/O Specification

USB PD BMC Receiver Normative Requirements

Name	Description	Min	Typ.	Max	Unit
cReceiver	CC receiver capacitance	200		600	pF
nTransitionCount	Transitions for signal detect	3			
tRxFilter	Rx bandwidth limiting filter (digital or analog)	100			ns
tTransitionWindow	Time window for detecting non-idle	12		20	Us
zBmcRx	Receiver Input Impedance	1			MΩ
vNoiseActive	Noise amplitude when BMC is active.			165	mV
vNoiseIdle	Noise amplitude when BMC is idle.			300	mV
vIRDropGNDC	Cable Ground IR Drop			250	mV

Table 6 USB I/O Specification

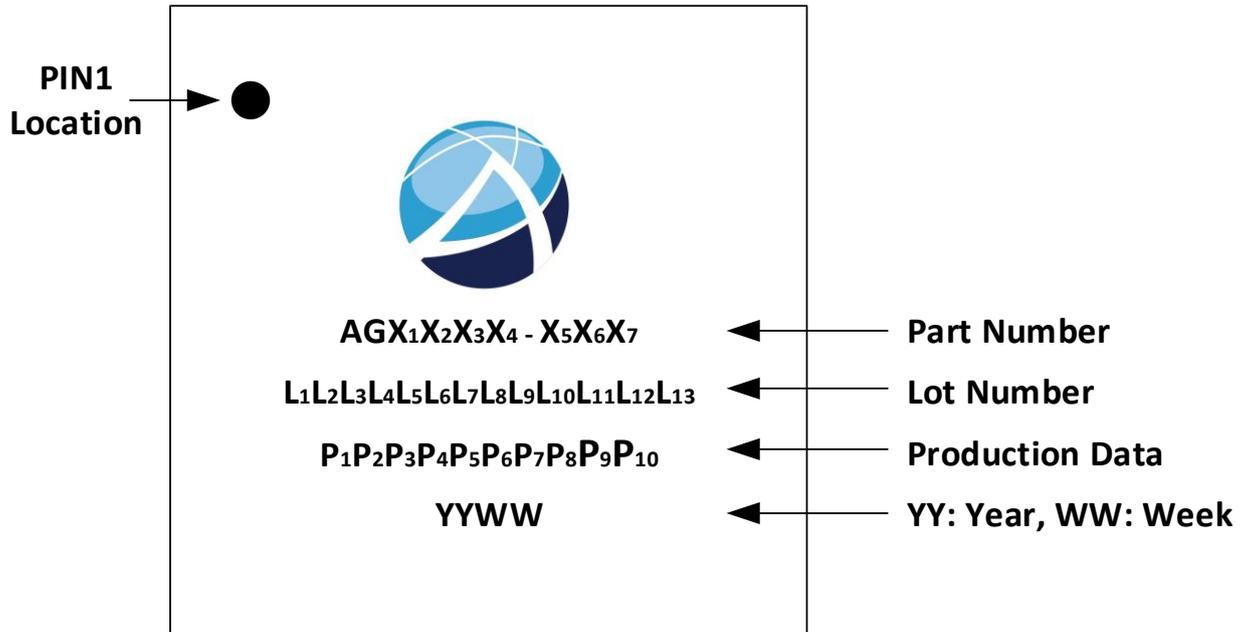
USB PD BMC Transmitter Normative Requirements

Name	Description	Min	Typ.	Max	Unit
tEndDriveBMC	Time to cease driving the line after the end of the last bit of the Frame.			23	us
tFall	Fall Time	300			ns
tHoldLowBMC	Time to cease driving the line after the final high-to-low transition.	1			us
tRise	Rise time	300			ns
vSwing	Voltage Swing	1.05	1.125	1.2	V
zDriver	Transmitter output impedance	33		75	Ω

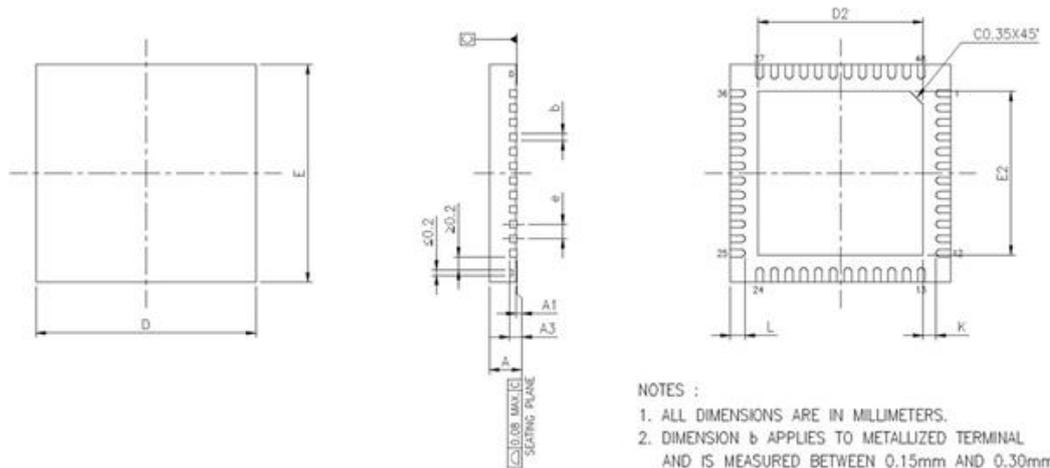
Table 7 USB PD Specification

VIII. Packing and Marking Specification

- Marking



● **Package Dimension**
AG9310-MBQ: QFN-48L 6x6mm



A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

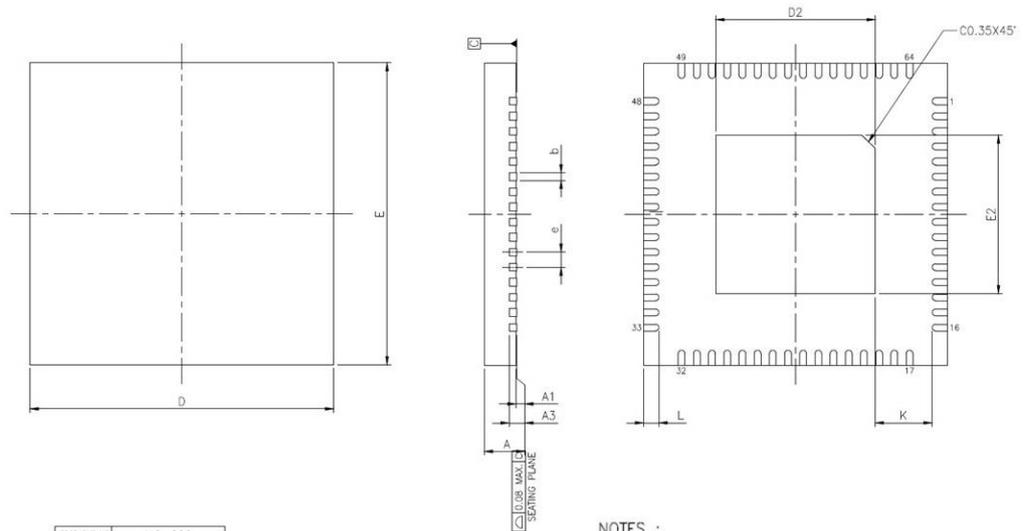
PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Sn	PPF	
185x18° ML	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	v	x	(W)VJJE-1

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 5 AG9310-MBQ Package Dimension

AG9310-MCQ: QFN-64L 8x8mm



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X864)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
268X26* ML	6.40	6.50	6.60	6.40	6.50	6.60	V	X	W(V)LLE-2

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 6 AG9310-MCQ Package Dimension

IX. References

- DisplayPort™ Standard 1.2b Specification
- HDMI 1.4b Specification

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