



ALGOLTEK

安格科技股份有限公司

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Datasheet

of

AG7210 Series

(HDMI 2.0 3:1 Switch)

Revision 1.2

2020/3/16

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Contents

I.	Feature	4
II.	General Description	5
III.	Functional Description	6
A.	High Definition Multimedia Interface (HDMI)	6
B.	Digital Visual Interface (DVI).....	6
C.	Input Selection Guideline.....	6
D.	Input Equalization Ratio.....	7
IV.	Pinouts and Pin Description	8
A.	Pin Diagram	8
B.	Pin Description.....	9
V.	Electrical Characteristics.....	11
A.	Absolute Maximum Ratings.....	11
B.	Operating Conditions	11
1.	General operating conditions.....	11
2.	Supply current characteristics	11
3.	I/O port characteristics.....	12
VI.	Terms and Abbreviations.....	13
VII.	Package Information	14
A.	LQFP-64L (7x7x1.6 mm ³ , pitch 0.4 mm).....	14
VIII.	Marking Information	15
IX.	Revision History	16

List of tables

Table 1. Pin description.....	9
Table 2. Voltage characteristics	11
Table 3. Thermal characteristics	11
Table 4. ESD characteristics.....	11
Table 5. Electrical sensitivities	11
Table 6. General operating conditions	11
Table 7. Typical current consumption	12
Table 8. I/O static characteristics	12
Table 9. Terms and Abbreviations.....	13
Table 10. Revision History	16

List of figures

Figure 1. Application illustration	4
Figure 2. System block diagram	5
Figure 3. LQFP-64 Pinout.....	8
Figure 4. LQFP-64 package outline.....	14
Figure 5. Marking information.....	15

I. FEATURE

- HDMI and DVI
 - HDMI 2.0b compliance
 - Up to 6Gbps TMDS bit rate
 - Up to 4096x2160p/30Hz resolution
- Support DC coupling for HDMI.
- Support integrated 50-ohm termination resistors for high-speed input signals
- Support output swing adjustment and pre-emphasis enhancement
- Support programmable equalization ratio for adjusting video quality and cable length
- Support automatic input selection of HDMI
- Support manual selection between active inputs
- Support external controller for input selection
- Support deep color and RGB/YUV (4:4:4), YUV (4:2:2) and YUV (4:2:0) color format
- Embedded LDO regulator from 5V to 3.3V/1.2V

- Operating characteristic
 - Operating voltage: 3.8V – 5.5V
 - Operating temperature: -40°C to 70°C
 - ESD HBM 8 kV
- Package
 - LQFP-64L 7x7x1.6 mm³

Application

- Media player
- Set-top Box
- Game console
- Television
- Monitor

Series	Part Number
AG7210	AG7210-MAL

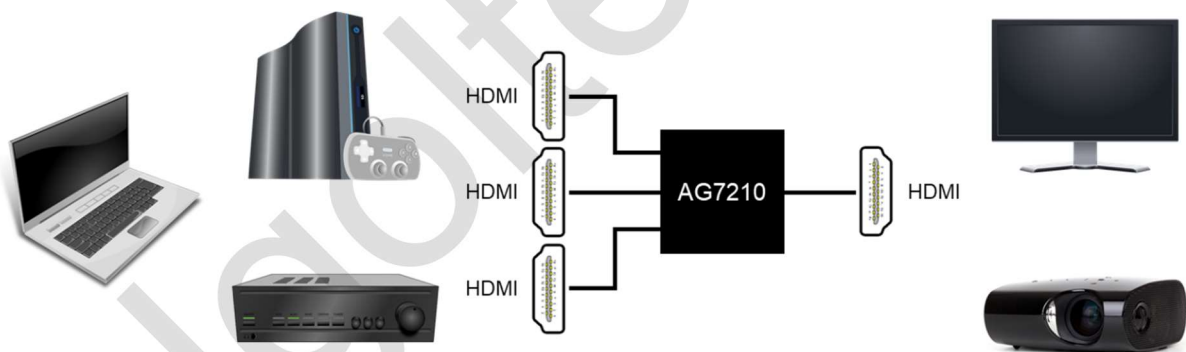


Figure 1. Application illustration

II. GENERAL DESCRIPTION

ALGOLTEK AG7210 series provide a switch functionality that allows up to three HDMI or DVI video streams to be transported to one display sink device.

HDMI is compliant with HDMI 2.0b Specification and supports up to 4096x2160/60Hz resolution. DVI supports up to 1920x1200/60Hz resolution. The maximum supported TMDS bit rate is 6Gbps and the maximum total throughput is 14.4 Gbps (4.8 Gbps/channel).

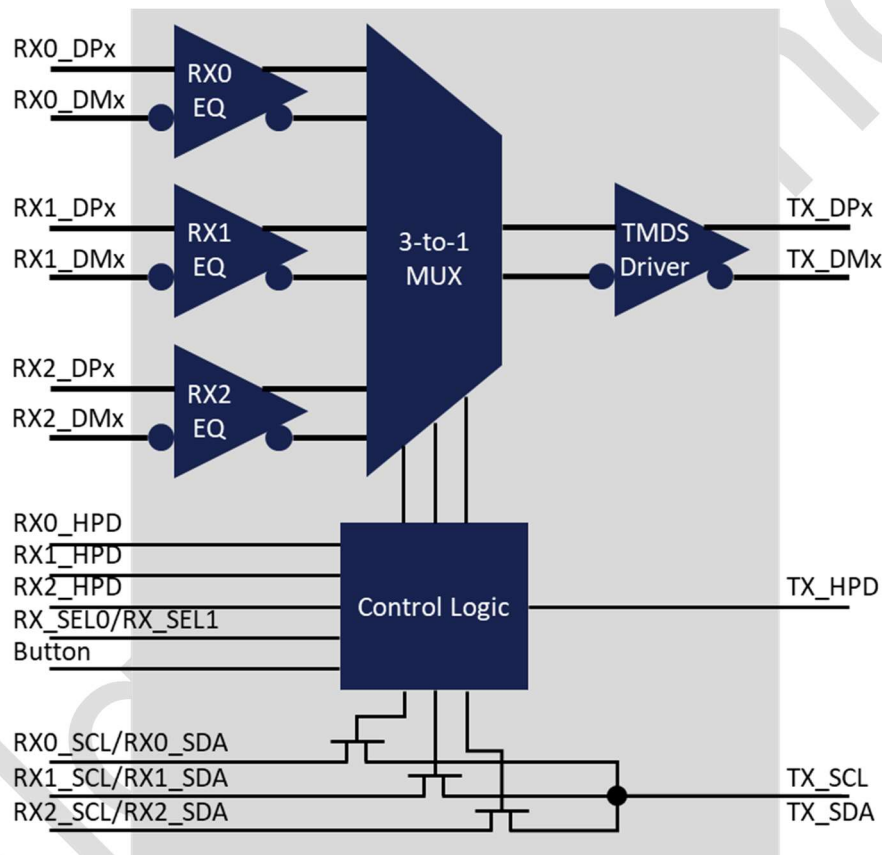


Figure 2. System block diagram

III. FUNCTIONAL DESCRIPTION

A. High Definition Multimedia Interface (HDMI)

AG7210 series supports HDMI video stream, compliant with HDMI 2.0 Specification. HDMI protocol allows each color channel to transfer individual RGB colors, audio data and auxiliary data between source and sink devices. The video transmission format is based TMDS encoding and the binary data is encoded with 8b/10b algorithm.

HDMI 2.0 specification allows TMDS bit rate up to 6 Gbps and TMDS clock rate to be 1/40 of the TMDS Bit Rate, which is up to 150 MHz. The maximum total throughput is 14.4 Gbps (4.8 Gbps/channel).

AG7210 series provides the support of VESA or CEA resolution up to 4096x2160/60Hz.

B. Digital Visual Interface (DVI)

AG7210 series supports single link DVI video stream. A single link DVI connection consists of four TMDS links. Three of the links represent the RGB components (red, green, and blue) of the video signal for a total of 24 bits per pixel. The fourth link carries the pixel clock.

In single-link mode, the maximum TMDS clock rate is 165 MHz, enabling the support of VESA resolution up to 1920x1200/60Hz or CEA resolution up to 1920x1080p/60Hz.

C. Input Selection Guideline

Input is selected by *RX_SEL0*, *RX_SEL1* and *Button* pins.

[RX_SEL1:RX_SEL0] = 00: RX0 will be selected as input

[RX_SEL1:RX_SEL0] = 01: RX1 will be selected as input

[RX_SEL1:RX_SEL0] = 10: RX2 will be selected as input

[RX_SEL1:RX_SEL0] = 11: None will be selected as input

[RX_SEL1:RX_SEL0] = floating: *Button* pin will be used as input selection control

D. Input Equalization Ratio

$RX_EQ\#$ pin and the value of resistor, connected between *Button* pin and ground, will define the ratio of input equalization.

When $RX_EQ\#$ is set to HIGH with different resistor:

Resistor (k Ω)	floating	75 ($\pm 5\%$)	10 ($\pm 5\%$)	27 ($\pm 5\%$)
Ratio (dB)	5	7.4	10	12.5

When $RX_EQ\#$ is set to HIGH with different resistor:

Resistor (k Ω)	27	other
Ratio (dB)	15	Not recommended

IV. PINOUTS AND PIN DESCRIPTION

A. Pin Diagram

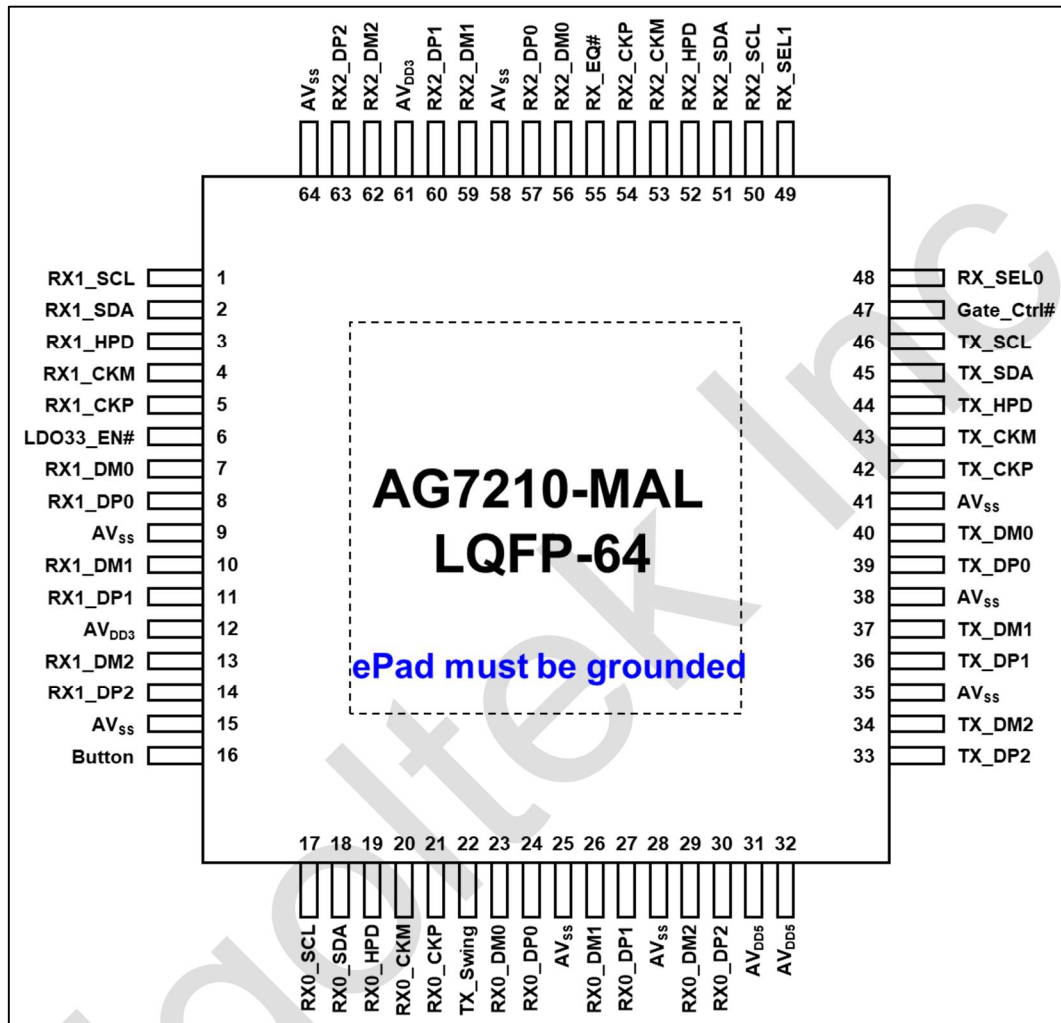


Figure 3. LQFP-64 Pinout

B. Pin Description

Table 1. Pin description

LQFP 64	Pin Name	Type	Description
1	RX1_SCL	I/O	I ² C serial clock for DDC of RX1
2	RX1_SDA	I/O	I ² C serial data for DDC of RX1
3	RX1_HPD	O	RX1 Hot-Plug Detect (HPD)
4	RX1_CKM	I	TMDS RX1 negative clock input
5	RX1_CKP	I	TMDS RX1 positive clock input
6	LDO33_EN#	I	Enable internal 5V to 3.3V LDO. Active low. [Default]
7	RX1_DM0	I	TMDS RX1 channel 0 negative data input
8	RX1_DP0	I	TMDS RX1 channel 0 positive data input
9	AV _{SS}	P	Ground pin for system
10	RX1_DM1	I	TMDS RX1 channel 1 negative data input
11	RX1_DP1	I	TMDS RX1 channel 1 positive data input
12	AV _{DD3}	P	3.3V analog power for decoupling capacitor
13	RX1_DM2	I	TMDS RX1 channel 2 negative data input
14	RX1_DP2	I	TMDS RX1 channel 2 positive data input
15	AV _{SS}	P	Ground pin for system
16	Button	I	Sequential RX input selection and EQ setting with internal pull-up resistor connected to AV _{DD5}
17	RX0_SCL	I/O	I ² C serial clock for DDC of RX0
18	RX0_SDA	I/O	I ² C serial data for DDC of RX0
19	RX0_HPD	O	RX0 Hot-Plug Detect (HPD)
20	RX0_CKM	I	TMDS RX0 negative clock input
21	RX0_CKP	I	TMDS RX0 positive clock input
22	TX_Swing	I	TX different swing adjustment with internal pull-up resistor connected to AV _{DD3} LOW: 950 mV (no pre-emphasis) HIGH: 1200 mV (2 dB pre-emphasis) [Default]
23	RX0_DM0	I	TMDS RX0 channel 0 negative data input
24	RX0_DP0	I	TMDS RX0 channel 0 positive data input
25	AV _{SS}	P	Ground pin for system
26	RX0_DM1	I	TMDS RX0 channel 1 negative data input
27	RX0_DP1	I	TMDS RX0 channel 1 positive data input
28	AV _{SS}	P	Ground pin for system
29	RX0_DM2	I	TMDS RX0 channel 2 negative data input
30	RX0_DP2	I	TMDS RX0 channel 2 positive data input
31	AV _{DD5}	P	5V supply voltage for analog circuit

LQFP 64	Pin Name	Type	Description
32	AV _{DD5}	P	5V supply voltage for analog circuit
33	TX_DP2	O	TMDS TX channel 2 positive data output
34	TX_DM2	O	TMDS TX channel 2 negative data output
35	AV _{SS}	P	Ground pin for system
36	TX_DP1	O	TMDS TX channel 1 positive data output
37	TX_DM1	O	TMDS TX channel 1 negative data output
38	AV _{SS}	P	Ground pin for system
39	TX_DP0	O	TMDS TX channel 0 positive data output
40	TX_DM0	O	TMDS TX channel 0 negative data output
41	AV _{SS}	P	Ground pin for system
42	TX_CKP	O	TMDS TX positive clock output
43	TX_CKM	O	TMDS TX negative clock output
44	TX_HPD	I	TX Hot-Plug Detect (HPD)
45	TX_SDA	I/O	I ² C serial data for DDC of TX
46	TX_SCL	I/O	I ² C serial clock for DDC of TX
47	Gate_Ctrl#	I/O	Gate control pin for PMOS
48	RX_SEL0	I	RX input selection
49	RX_SEL1	I	RX input selection
50	RX2_SCL	I/O	I ² C serial clock for DDC of RX2
51	RX2_SDA	I/O	I ² C serial data for DDC of RX2
52	RX2_HPD	O	RX2 Hot-Plug Detect (HPD)
53	RX2_CKM	I	TMDS RX2 negative clock input
54	RX2_CKP	I	TMDS RX2 positive clock input
55	RX_EQ#	I	RX equalization ratio control
56	RX2_DM0	I	TMDS RX2 channel 0 negative data input
57	RX2_DP0	I	TMDS RX2 channel 0 positive data input
58	AV _{SS}	P	Ground pin for system
59	RX2_DM1	I	TMDS RX2 channel 1 negative data input
60	RX2_DP1	I	TMDS RX2 channel 1 positive data input
61	AV _{DD3}	P	3.3V analog power for decoupling capacitor
62	RX2_DM2	I	TMDS RX2 channel 2 negative data input
63	RX2_DP2	I	TMDS RX2 channel 2 positive data input
64	AV _{SS}	P	Ground pin for system

V. ELECTRICAL CHARACTERISTICS

A. Absolute Maximum Ratings

Table 2. Voltage characteristics

Symbol	Parameter	Min	Max	Unit
AV _{DD5} -V _{SS}	5V supply voltage for analog circuit	-0.5	6	V

Table 3. Thermal characteristics

Symbol	Parameter	Min	Max	Unit
T _A	Ambient temperature	-40	70	°C
T _J	Junction temperature	0	85	°C
T _{ST}	Storage temperature	-60	150	°C

Table 4. ESD characteristics

Symbol	Ratings	Conditions	Class	Max	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = 25°C conforming to JESD22-A114-B	3B	8	kV
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = 25°C conforming to JESD22-C101-C	III	500	V
V _{ESD(MM)}	Electrostatic discharge voltage (machine model)	T _A = 25°C conforming to JESD22-A115-C	B	350	V

Table 5. Electrical sensitivities

Symbol	Ratings	Conditions	Class	Max	Unit
LU	Static latch-up class	T _A = 25°C conforming to JESD78	I level B	400	mA

B. Operating Conditions

1. General operating conditions

Table 6. General operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
T _A	Ambient temperature	0	25	70	°C
AV _{DD5}	5V supply voltage for analog circuit	3.8	5	5.5	V

2. Supply current characteristics

The current consumption is a function of several parameters and factors including operating voltage, ambient temperature, enabled display terminal and display resolution.

Typical current consumption

AG7210 series is measured under following conditions:

- TMDS clock rate: 148.5 MHz
- TMDS bit rate: 5.94 Gbps
- $T_A = 25^{\circ}\text{C}$

Table 7. Typical current consumption

Symbol	Parameter	Conditions	Typ	Unit
I_{AVDD5}	Supply current of AV_{DD5} power line	$AV_{DD5} = 3.3\text{V}$	110	mA

3. I/O port characteristics

Table 8. I/O static characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	2.4		5.3	V
V_{OL}	Output Low Voltage	0		0.4	V
V_{IH}	Input High Voltage	2.0		5.3	V
V_{IL}	Input Low Voltage	0		0.8	V
I_{LI}	Input leakage current			± 1	μA

VI. TERMS AND ABBREVIATIONS

Table 9. Terms and Abbreviations

Acronym	Description
CEA	Consumer Electronics Association
CTA	Consumer Technology Association (Formerly CEA)
DDC	Display Data Channel
DVI	Digital Visual Interface
EDID	Extended Display Identification Data
HDMI	High Definition Multimedia Interface
I ² C	Inter-Integrated Circuit
I/O	Input/Output
MCCS	Monitor Control Command Set
TMDs	Transition Minimized Differential Signaling
VESA	Video Electronics Standards Association

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VII. PACKAGE INFORMATION

A. LQFP-64L (7x7x1.6 mm³, pitch 0.4 mm)

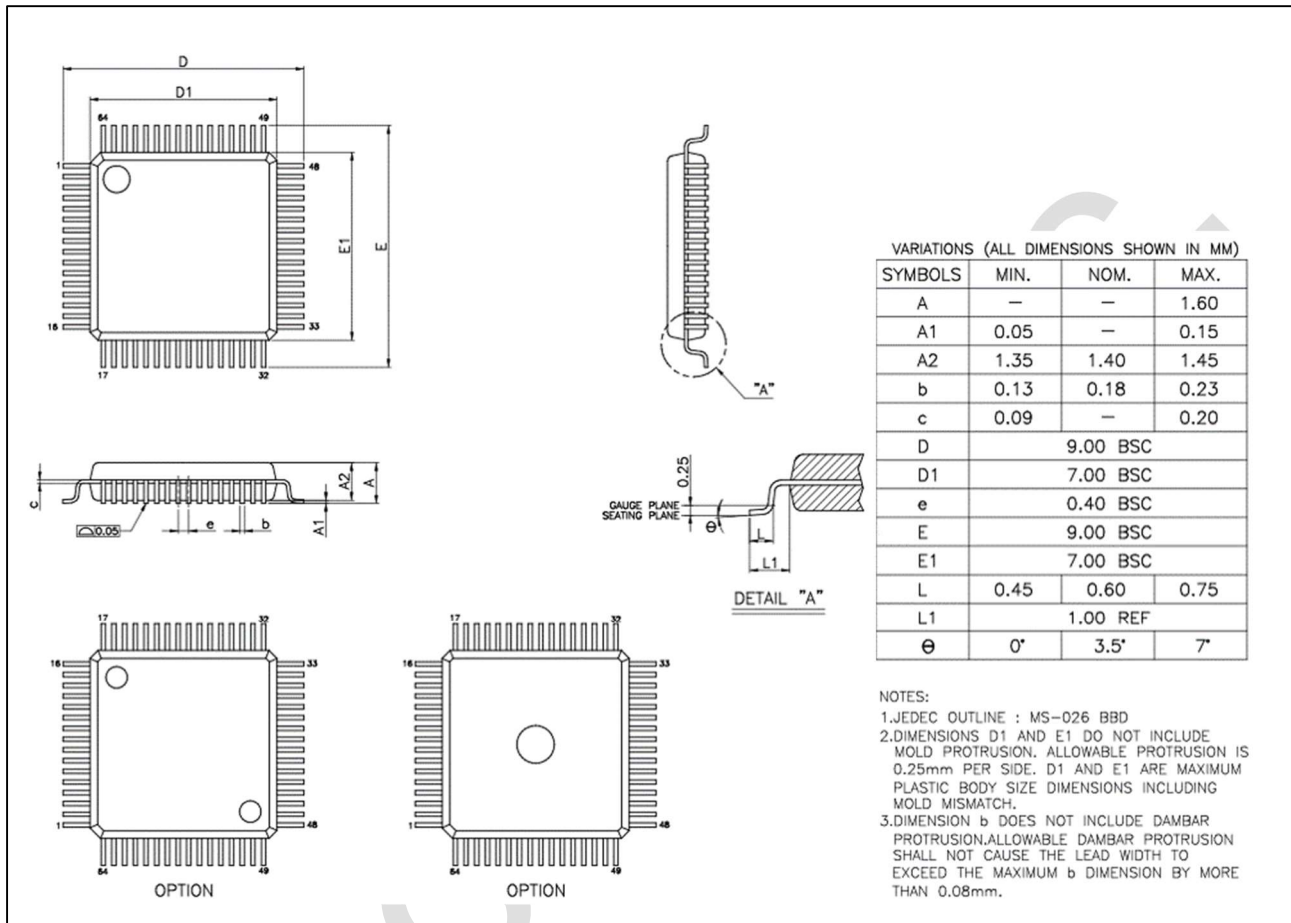


Figure 4. LQFP-64 package outline

VIII. MARKING INFORMATION

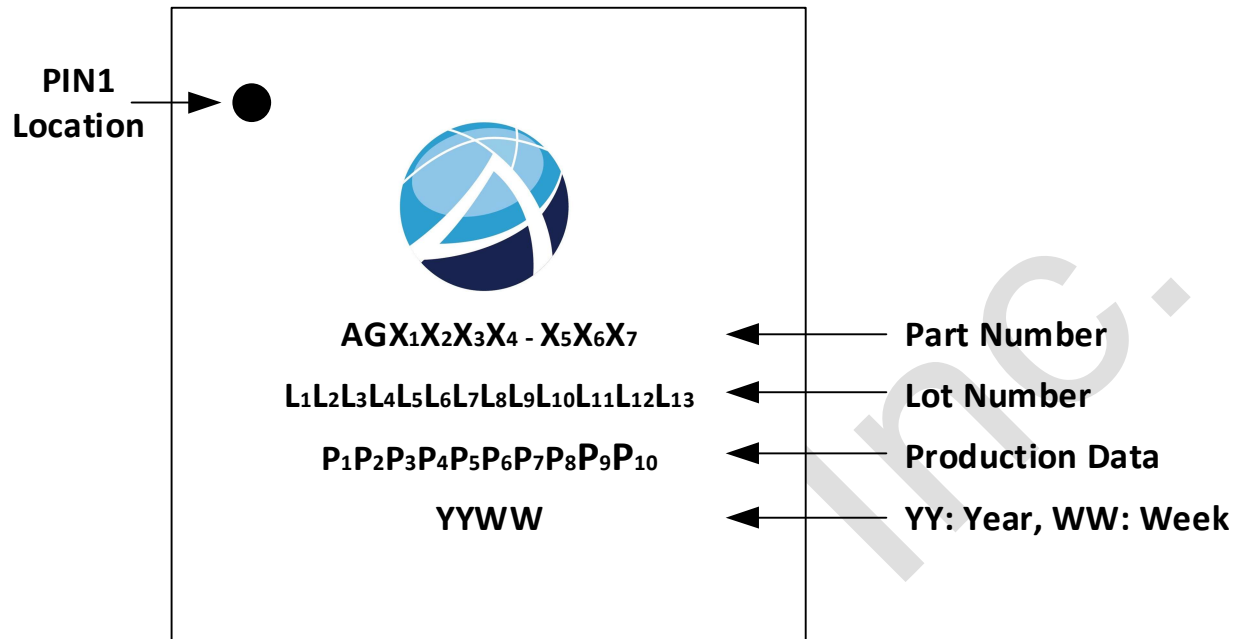


Figure 5. Marking information

IX. REVISION HISTORY

Table 10. Revision History

Date	Revision	Remark
2017/11/14	1.0	Initial release
2018/12/18	1.1	Update T _A value
2020/03/16	1.2	Revise content

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