

用于卫星通信、雷达电子战以及5G 无线通信的相控阵设计解决方案

April 20, 2017

售后支持: 8008100189 4004100189

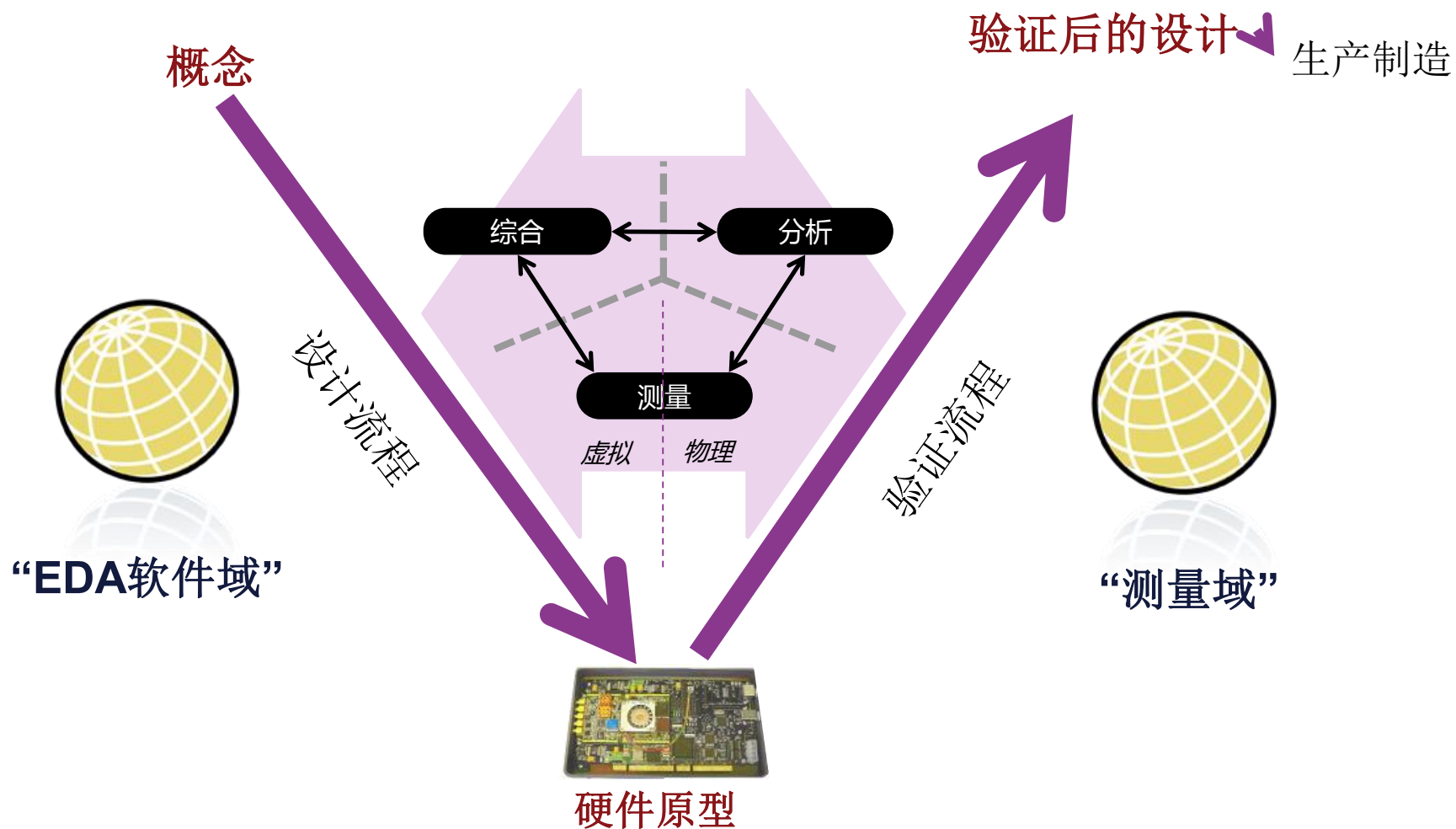
eesof-asia_support@Keysight.com

应用视频: http://v.youku.com/v_show/id_XNzU1MDAwOTYw.html?f=22614819&from=y1.7-3

软件应用技巧: http://www.keysight.com/find/ads_tips

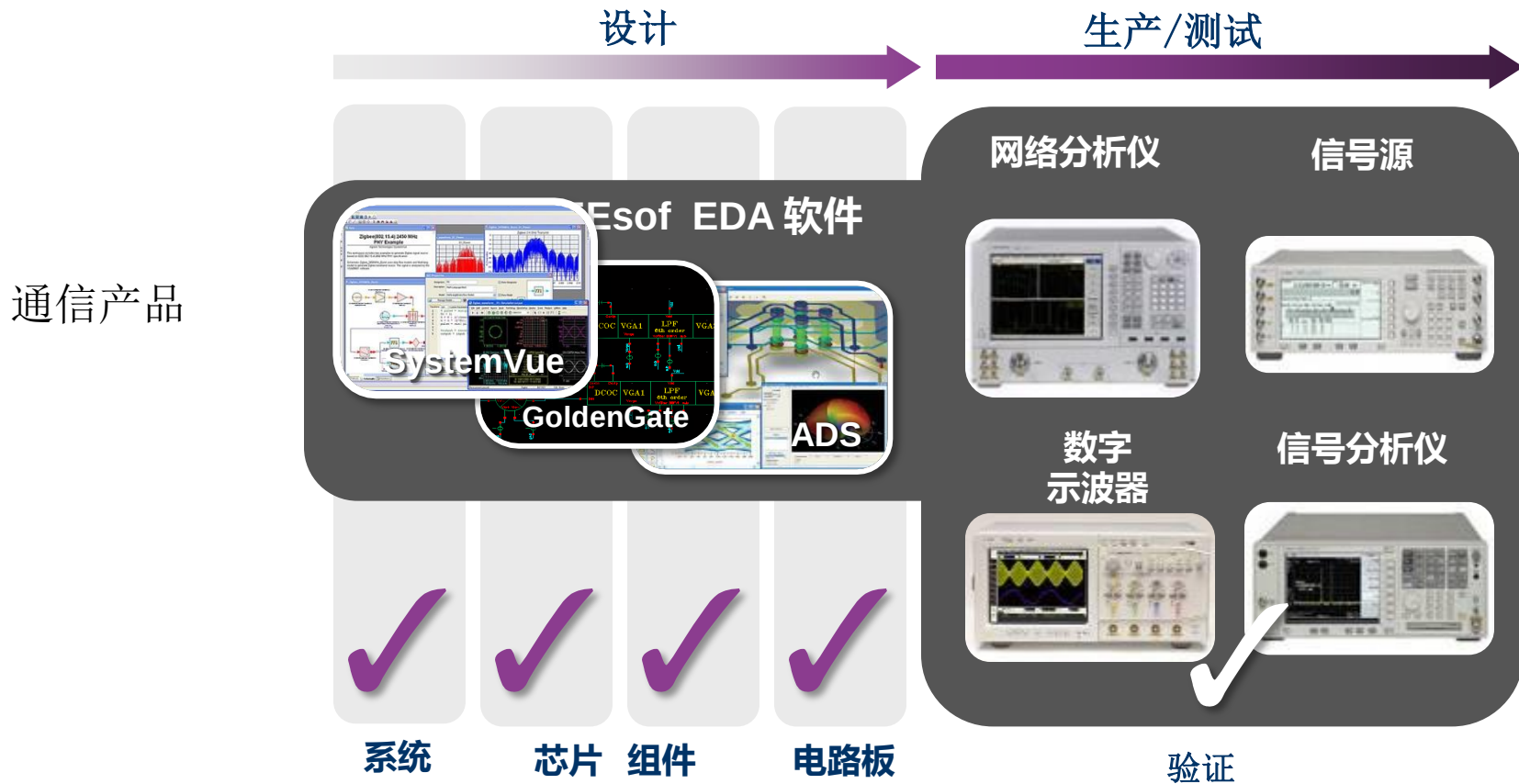
由概念转变为经验证的正确设计

加快设计成熟度尽早用于生产制造



Keysight EEsof EDA

不断创造先锋技术、加速通信成品的发展

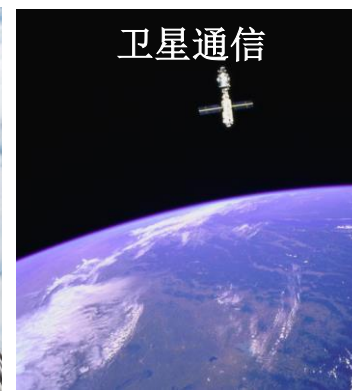
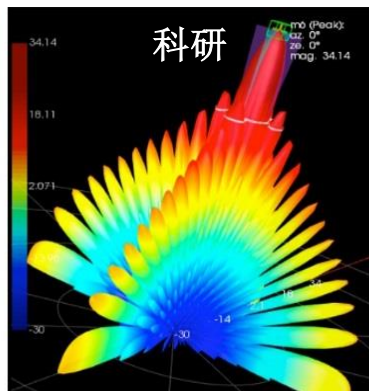
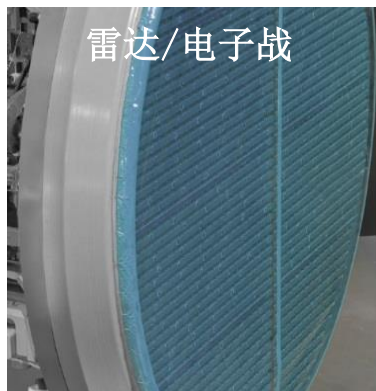


内容安排

- 相控阵系统设计面临的挑战
- 相控阵系统设计分析
- 相控阵单元电路设计
- 总结

相控阵系统发展的市场驱动力

- 目标：在较小的体积、重量和功耗条件下，以最低的资产和运行费用提供更高的服务水平



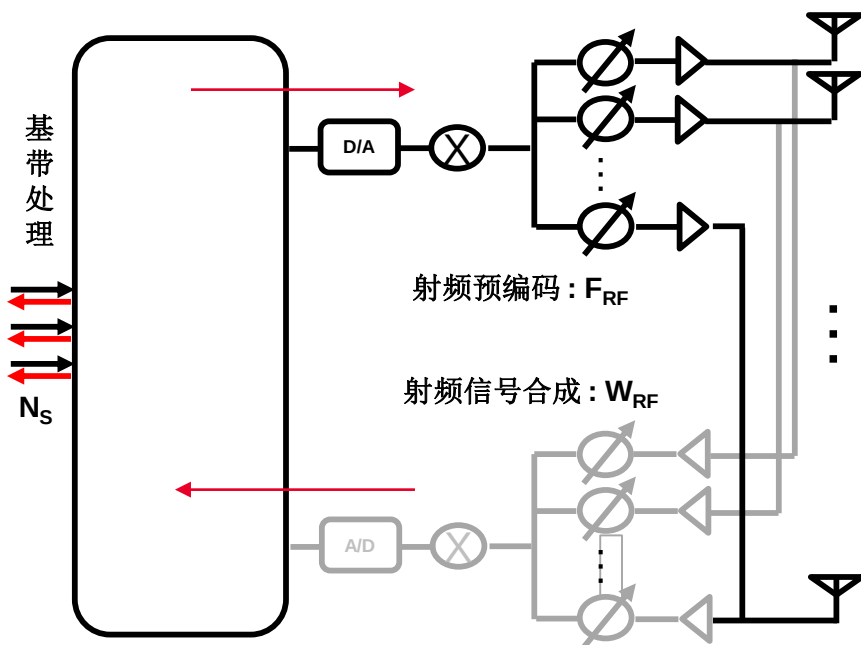
为什么使用波束成形技术？

- 降低干扰
- 增加距离
- 多用户，动态环境
- 提高安全性

为什么是现在？

- 半导体技术发展
- 服务的需要
- 毫米波频段波长更短

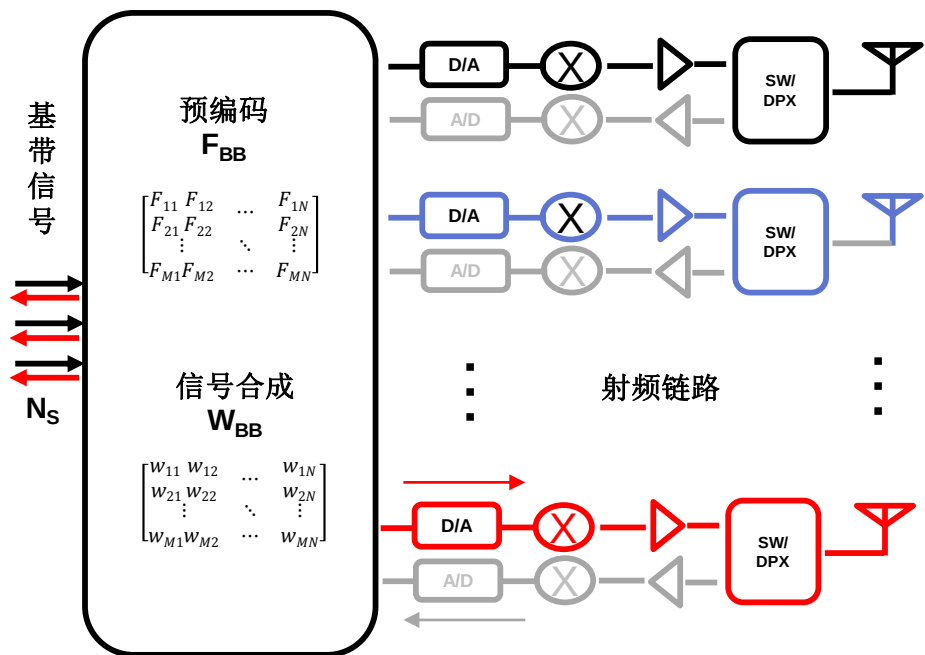
相控阵系统的实现：射频/模拟波束成形



在射频进行波束成形(幅度/相位控制)

- 单路基带信号
 - 只适合于单流 (相比MIMO)
 - 低功耗, 系统复杂性
 - 对于毫米波电路, 只需要一个上下变频电路
 - 接收电路信号处理增益 (提高SNR)
- 模拟移相电路
 - 幅度恒定限制
 - 移相分辨率

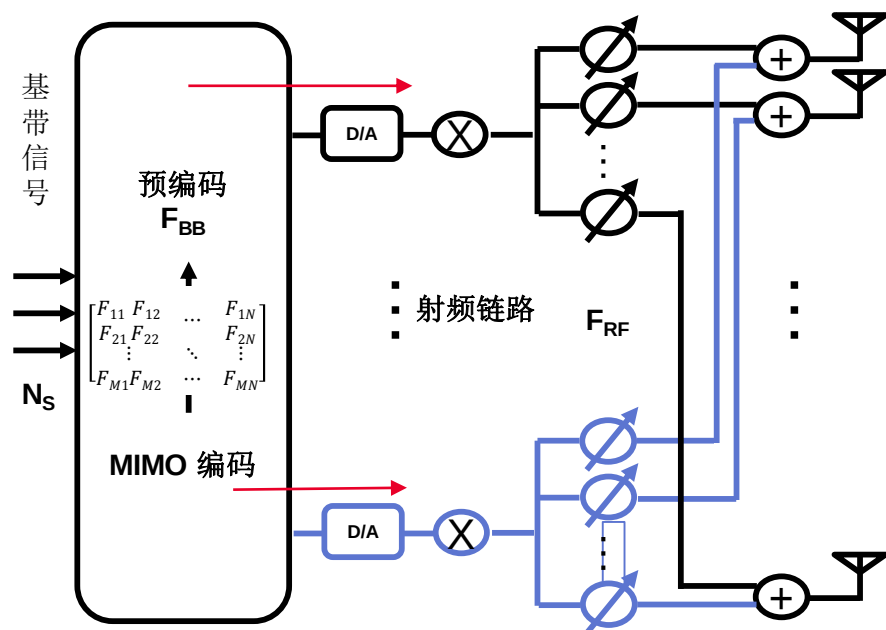
相控阵系统的实现：数字波束成形



在基带进行波束成形(幅度/相位控制)

- 每个通道使用 ADC/DAC
 - 硬件复杂性
 - 功耗（直流，发热）
 - “N” 个独立的射频上下变频通道
- 更高的波束成形增益
- 支持多流多用户
- 灵活的传输模式

相控阵系统的实现：混合波束成形



在基带进行幅度控制 (MIMO/Tapers)
在射频进行相位控制 (每个波束方向)
在射频进行多波束相加 (每个天线)

- 降低硬件复杂性
- 性能接近DBF架构
- 5G 应用

相控阵系统设计的挑战：多域设计

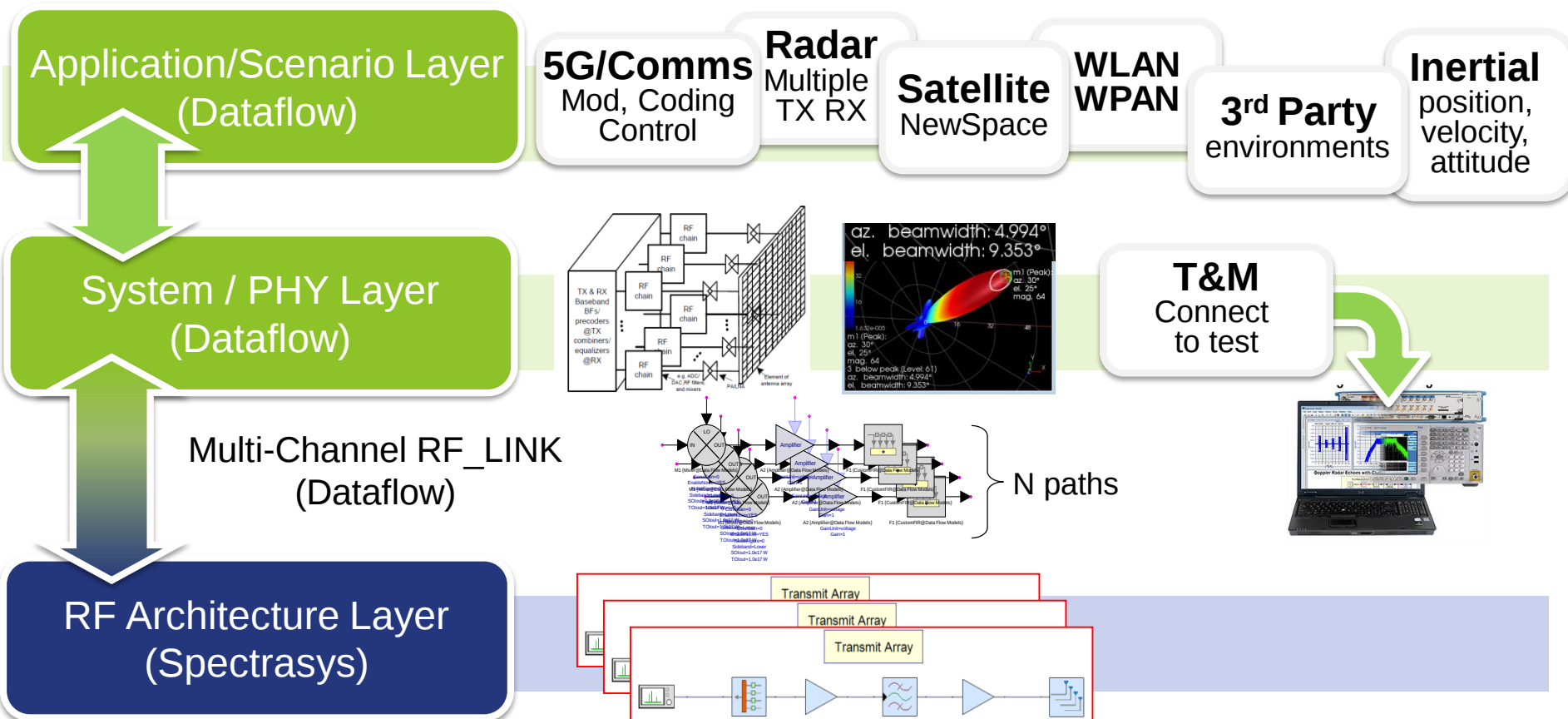
– “有多少工程师是为相控阵子系统设计服务的？”



- 多少种不同的工具？
- 多少种不同的数据格式？
- 在什么时候能将这些设计集成起来？
- 如何在不同的设计域中快速发现/跟踪问题？

相控阵系统架构设计流程

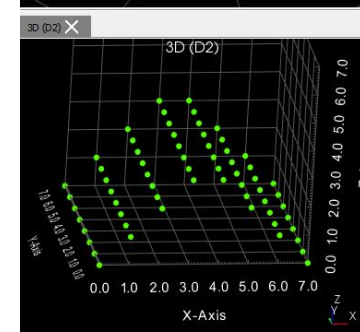
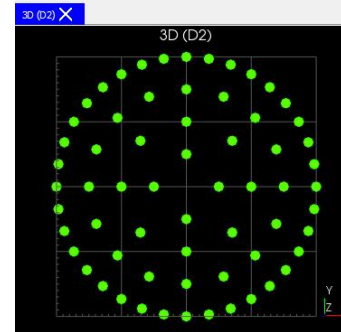
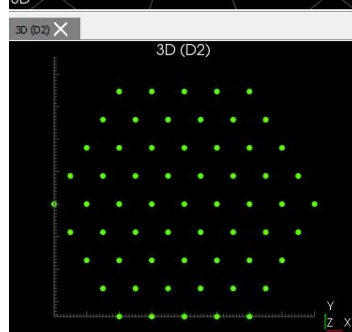
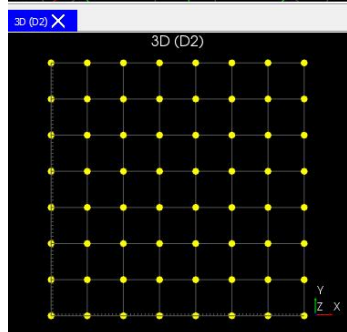
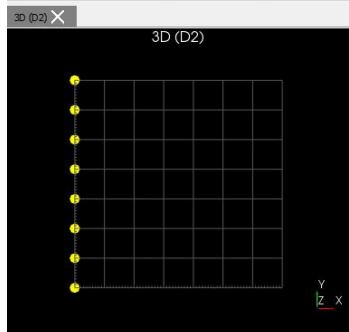
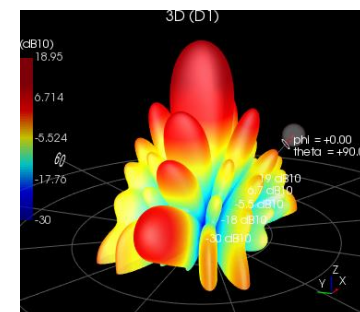
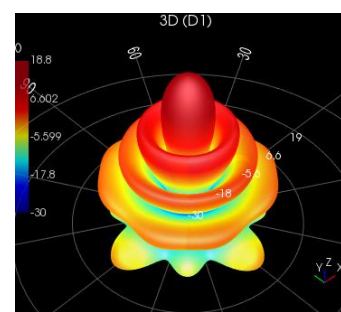
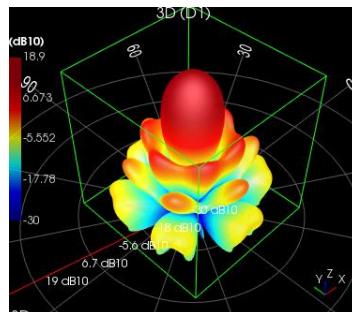
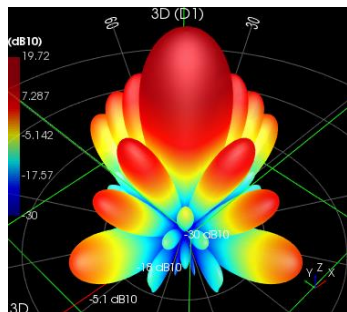
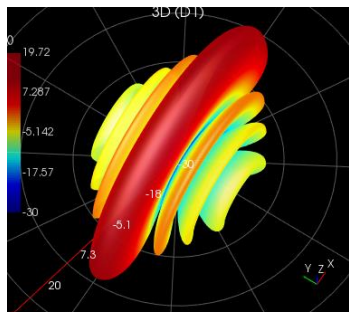
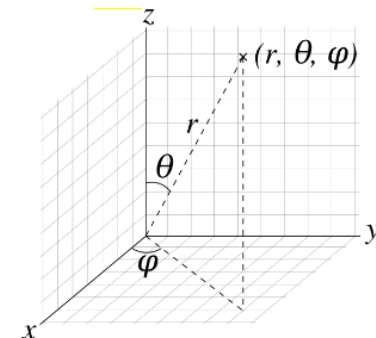
- A common “cockpit” across multiple disciplines : BB, RF, System, Application, T&M



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阵列设置、波束显示与测量



等距线阵

矩形阵

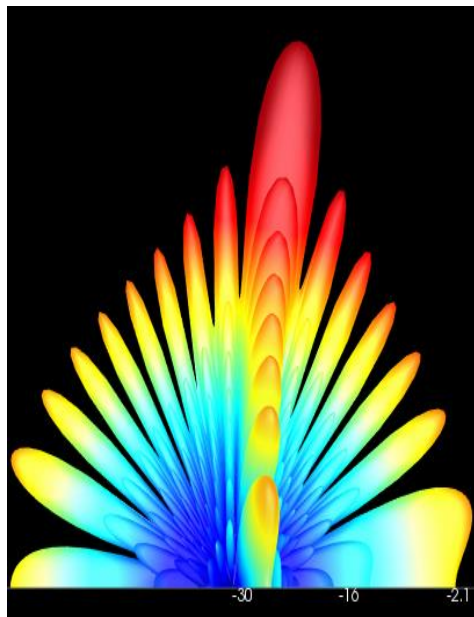
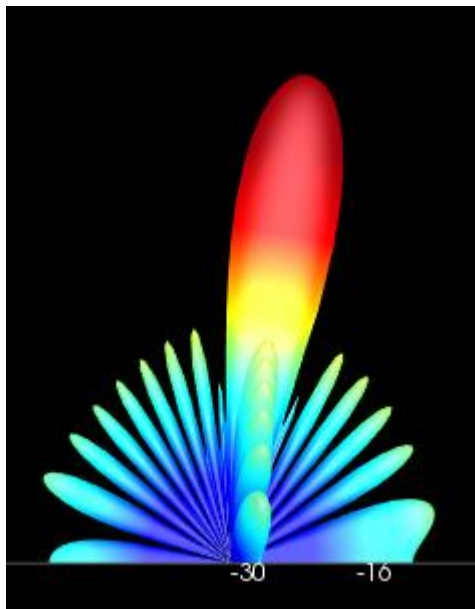
三角阵

圆阵

三维/共形阵

阵列设置、波束显示与测量

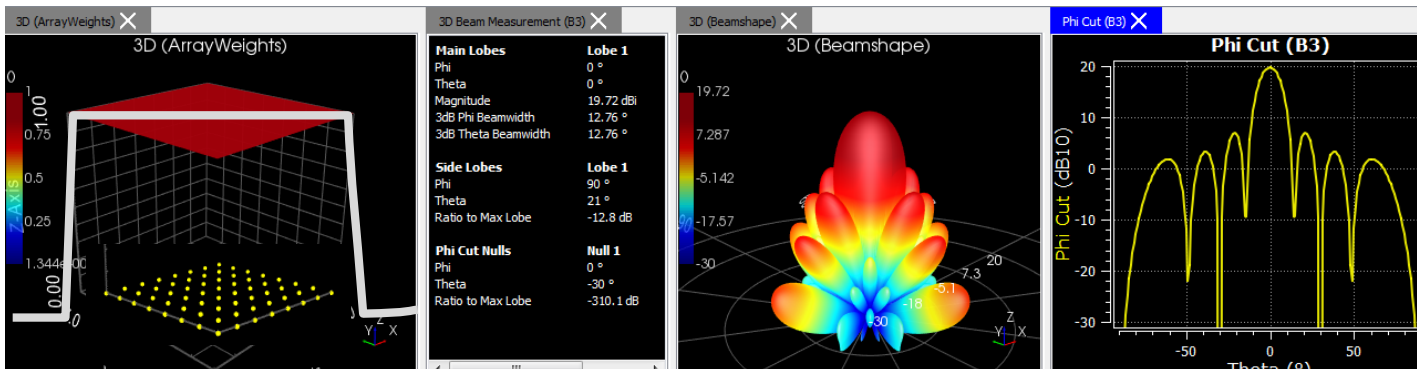
旁瓣控制



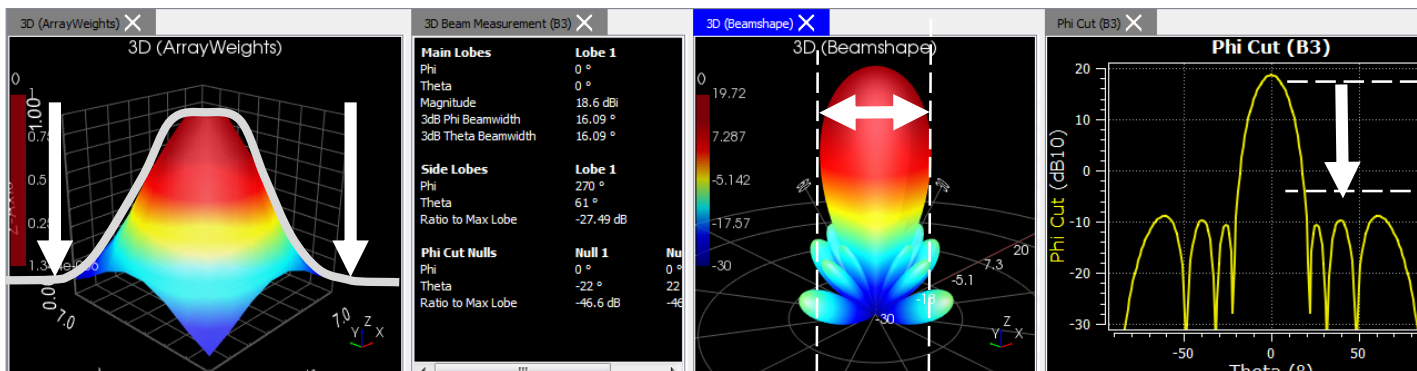
阵列设置、波束显示与测量

加窗处理

不加窗



二维
泰勒窗



旁瓣抑制
-12.8dBc
--> -27.5dBc

主瓣展宽
12.8° → 16.1°

波束扫描 ---主瓣宽度 旁瓣抑制

$\Theta=0^\circ$

$\Theta=15^\circ$

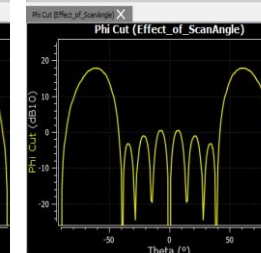
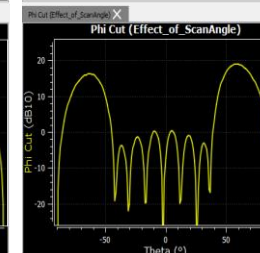
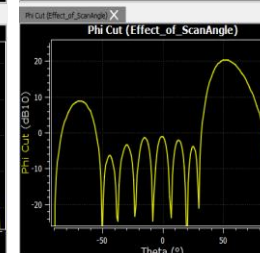
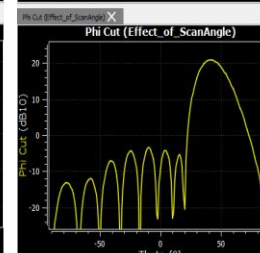
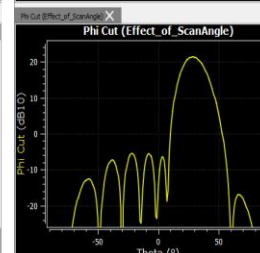
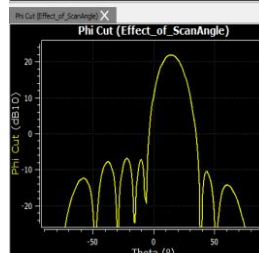
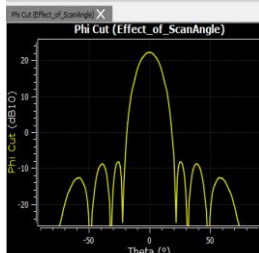
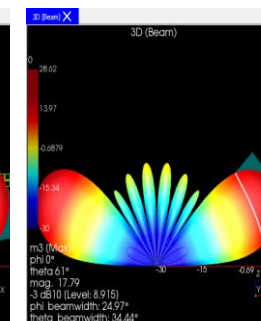
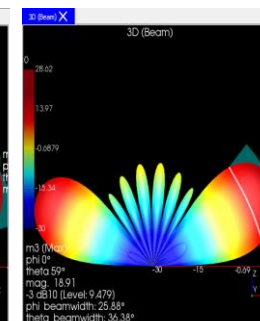
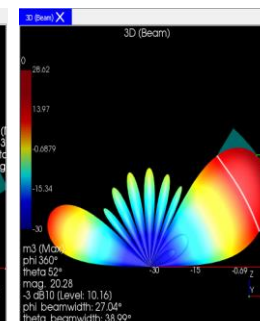
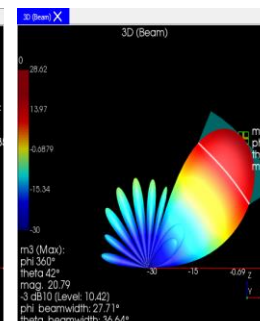
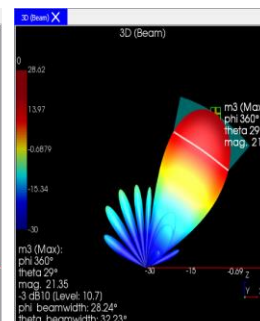
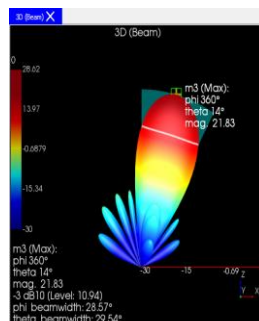
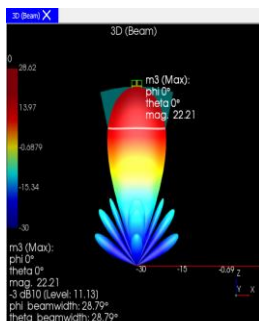
$\Theta=30^\circ$

$\Theta=45^\circ$

$\Theta=60^\circ$

$\Theta=75^\circ$

$\Theta=90^\circ$



BW=28.8°

BW=29.4°

BW=32.3°

BW=36.6°

BW=39.0°

BW=36.4°

BW=34.4°

SLL= -30.3dB

SLL= -28.6dB

SLL= -26.5dB

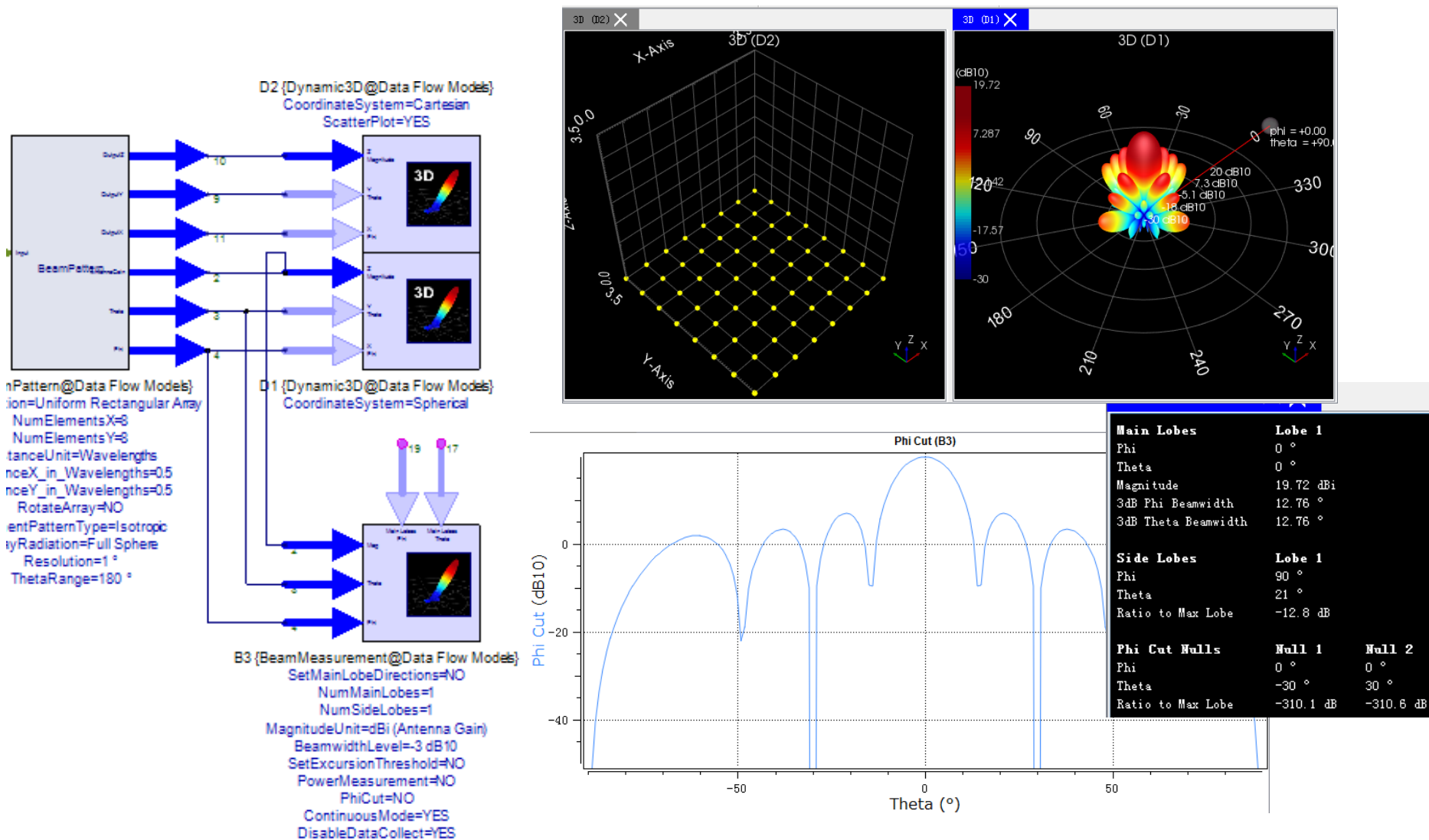
SLL= -23.7dB

SLL= -11.3dB

SLL= -2.7dB

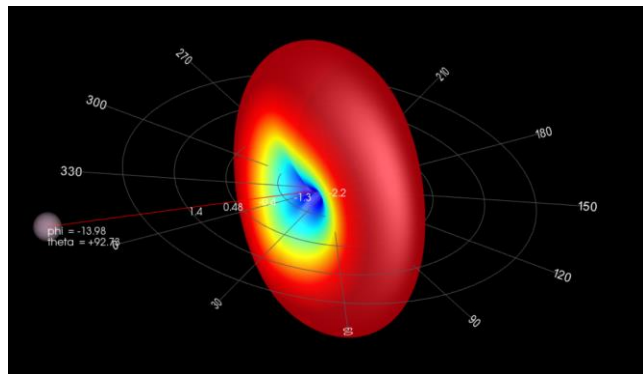
SLL= 0 dB

SystemVue 波束合成与显示



波束合成实例：

单天线阵元方向图



SystemVue 显示结果

天线阵列配置：

8x4 矩形天线阵

阵元间距：~0.6 波长

仿真步骤：

配置天线阵列形式及间距

指定天线方向图文件

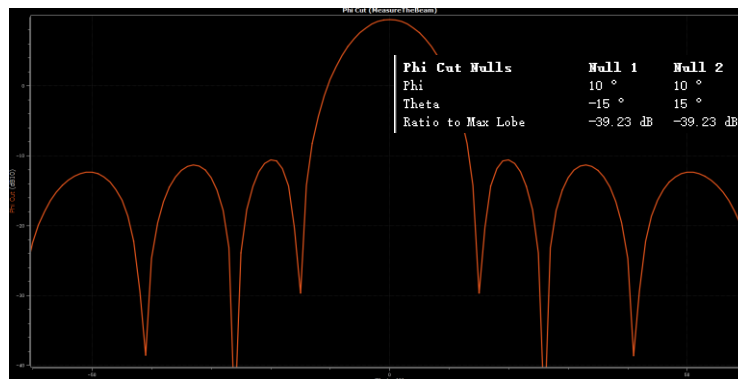
设定合成波束方向

运行仿真，显示合成波束及信息

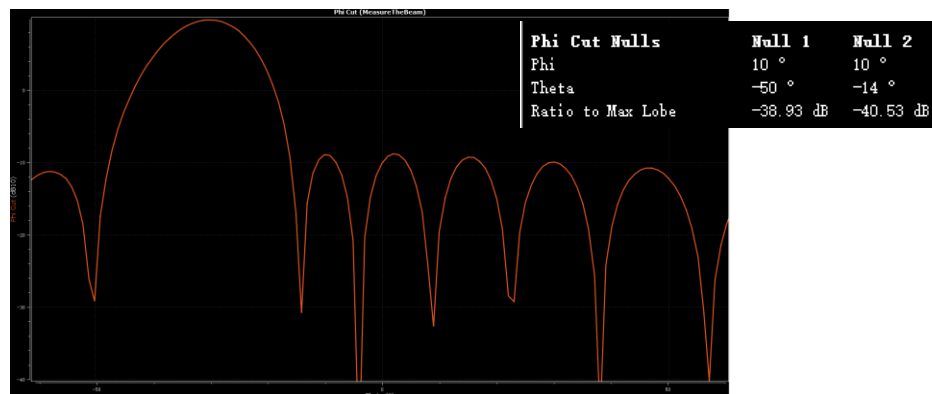
波束合成实例(仿真):

二维波束切面比较 (水平方向8天线阵元)

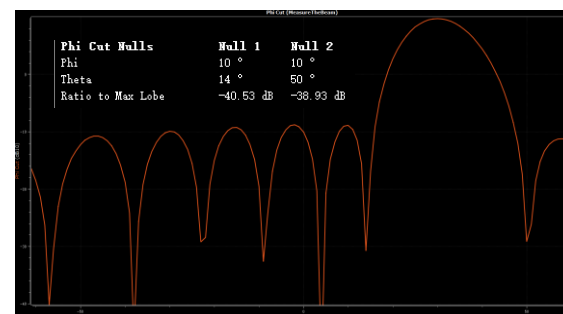
仿真结果 (0 degree)



仿真结果(-30 degree)



仿真结果 (30 degree)



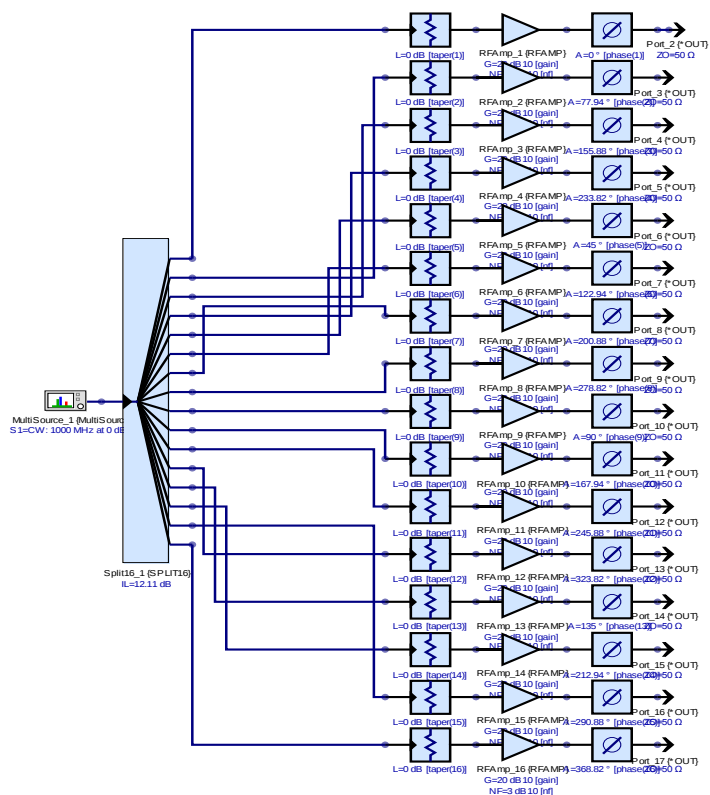
波束合成实例(仿真与实测结果对比):

波束方向	3dB 波束宽度 (Degree)		第一零点 (左) (Degree)		第一零点 (右) (Degree)		第一旁瓣 (左) (dB)		第一旁瓣 (右) (dB)	
	仿真	实测	仿真	实测	仿真	实测	仿真	实测	仿真	实测
0 degree	12.2	12.0	-15	-15	15	-14	-20	-19	-20	-18
30 degree	14.5	14.0	14	13	50	50	-20	-21	-20	-20
-30 degree	14.5	14.5	-50	-50	-14	-13	-20	-22	-20	-19

相控阵射频子系统建模与仿真

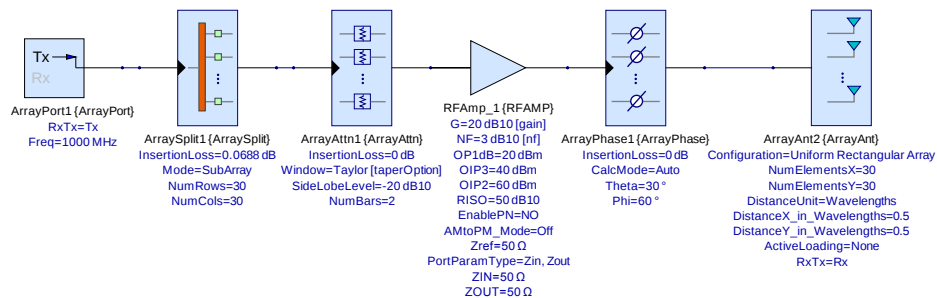
传统的射频子系统建模
SystemVue SpectraSys仿真

System1 (Design1)



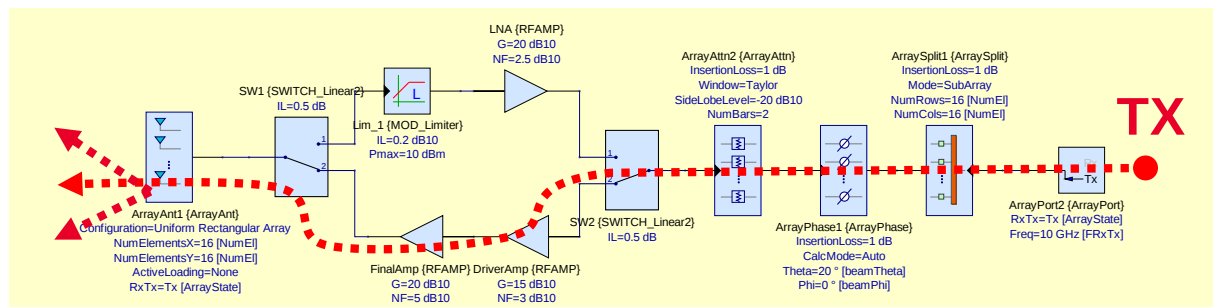
阵列射频系统
SystemVue PhaseArray仿真

PhasedArray2 (Design2)

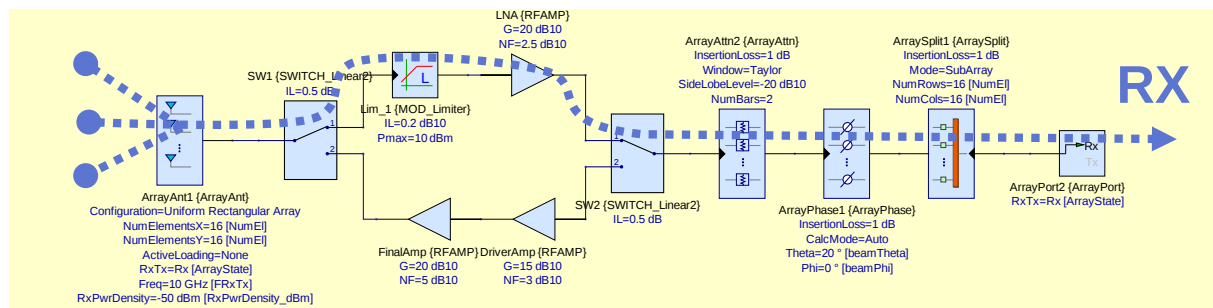


射频子系统建模

射频发射机及接收机



发射机
1路输入激励，“N”路输出



接收机

“N”路输入激励，1路输出

射频子系统建模

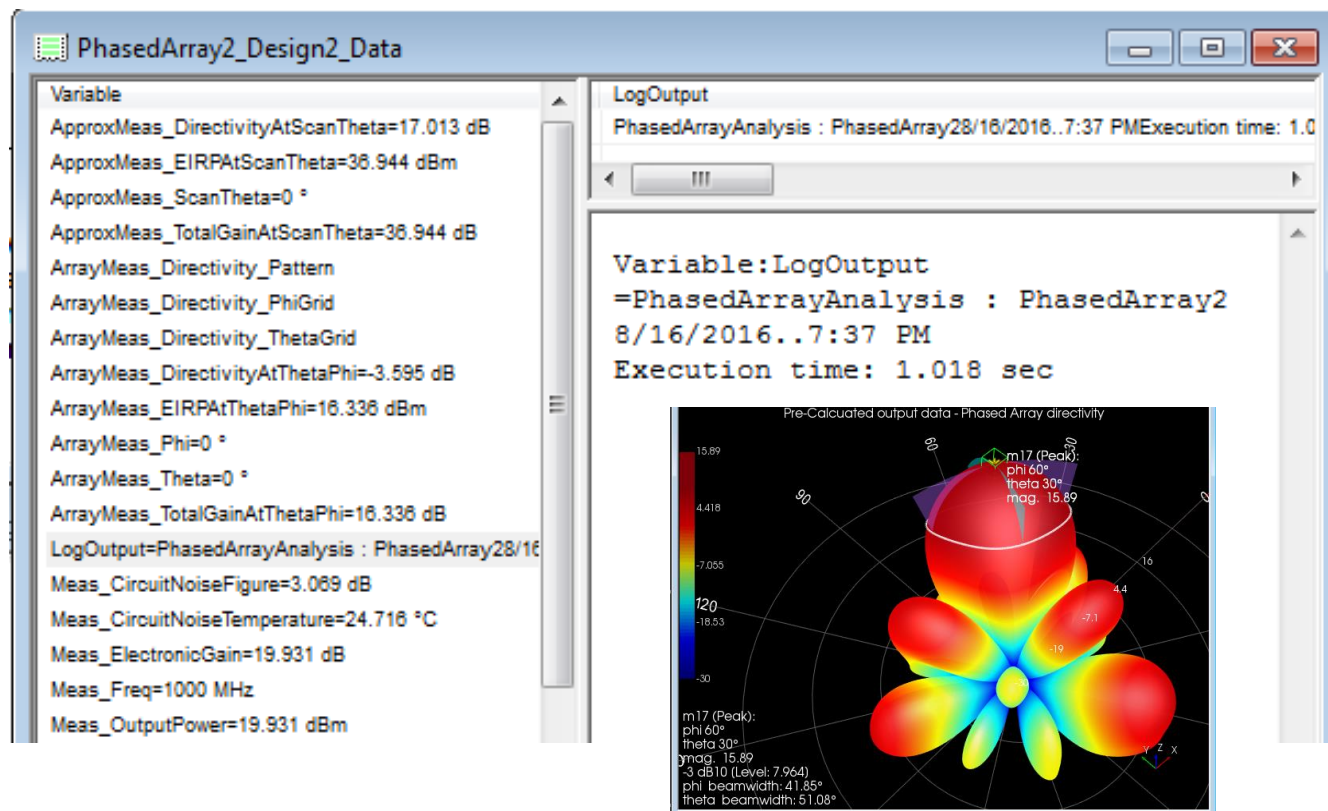
预定义测量功能

预定义阵列测量

- Gain/Tot (接收机)
- EIRP (发射机)
- 在指定 ($\phi_{\text{meas}}, \theta_{\text{meas}}$) 上的Gain, Directivity

三维绘图及光标功能

- Beam direction
- Beam width
- Sidelobes & nulls



射频部件性能对阵列合成方向图的影响

功放非线性

- 增益压缩
- 饱和
- AM-PM

部件性能偏差

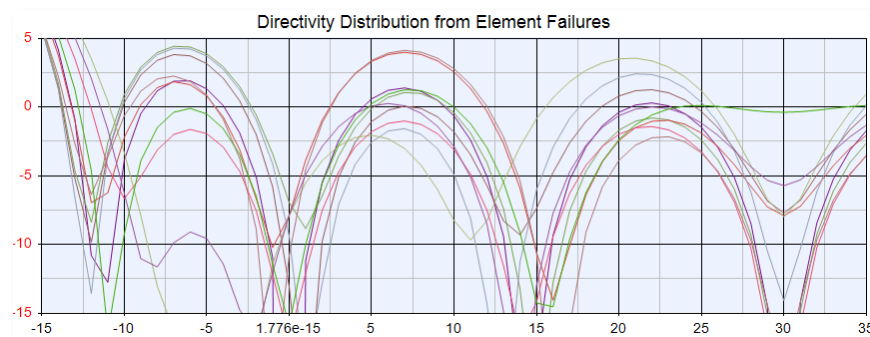
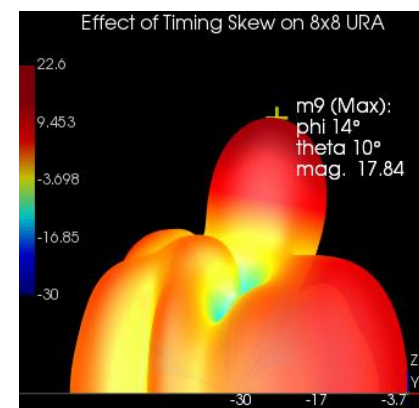
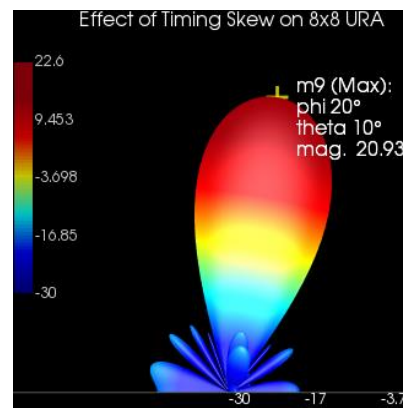
- 移相器/衰减器

量化影响

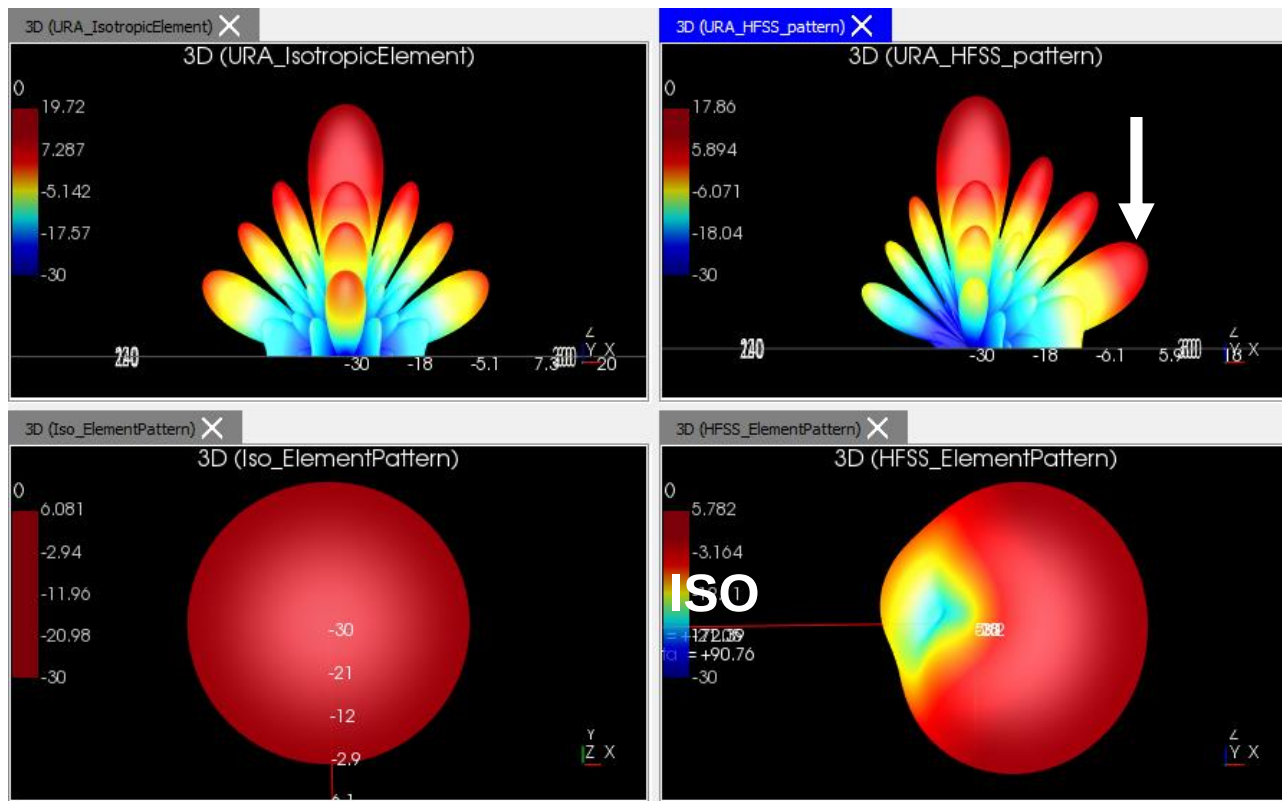
- 增益/相位

天线耦合及阵元方向图

部件性能统计特性



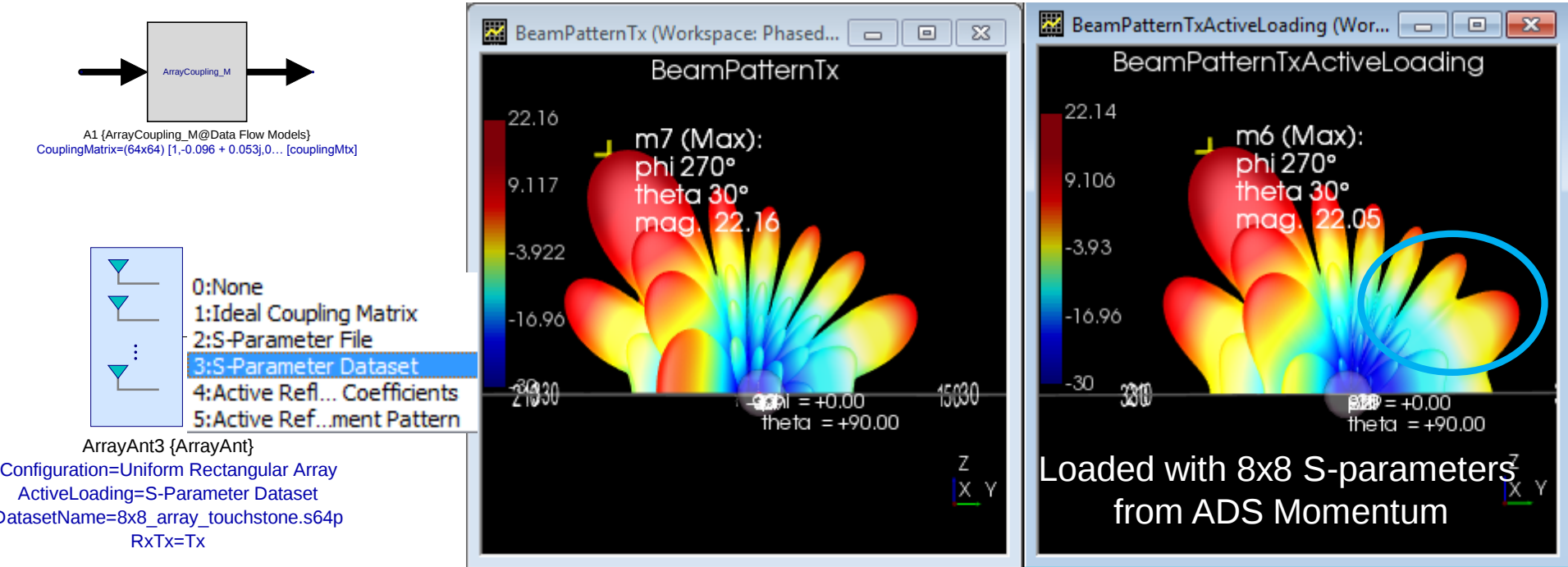
相控阵天线单元方向图的影响



- Imperfect element patterns express themselves at the beam level
- Coupling and loading can worsen internal mismatches
 - Beam degradation
 - Blind spots

相控阵天线单元有源负载及阵元耦合

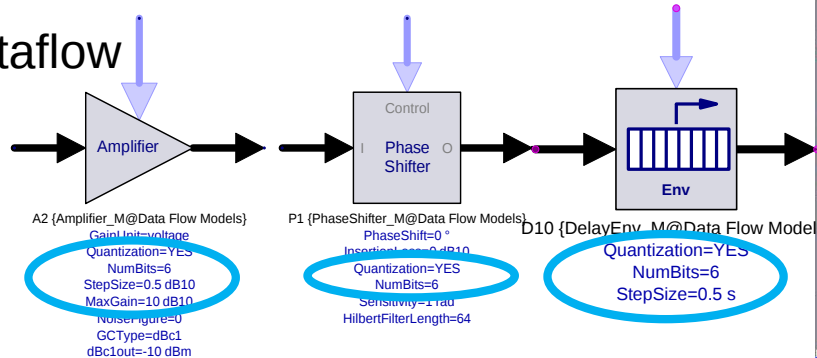
- Changes loading, beam pattern



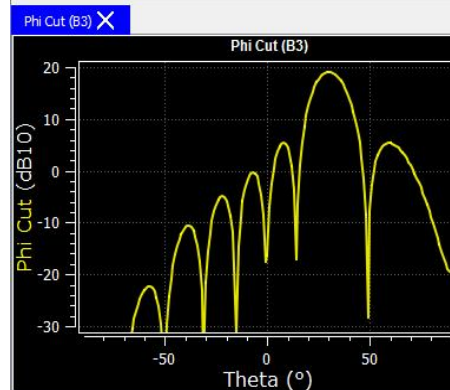
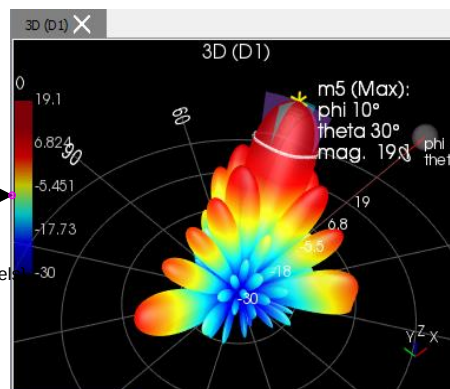
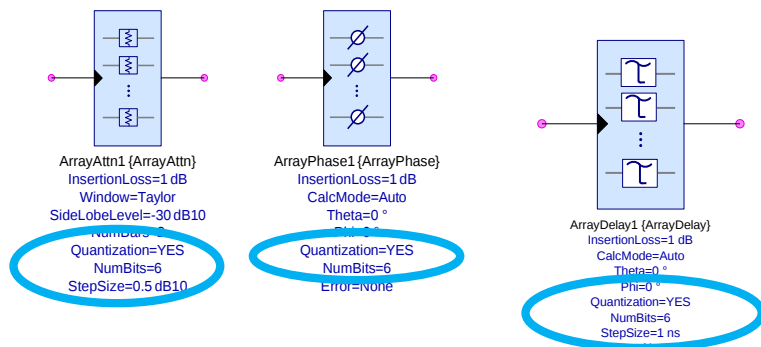
射频损伤：Gain & Phase/Delay Quantization

- Discrete-valued states limit beam accuracy and sidelobe levels

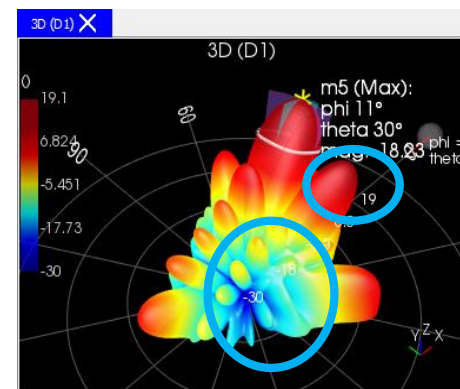
Dataflow



RF

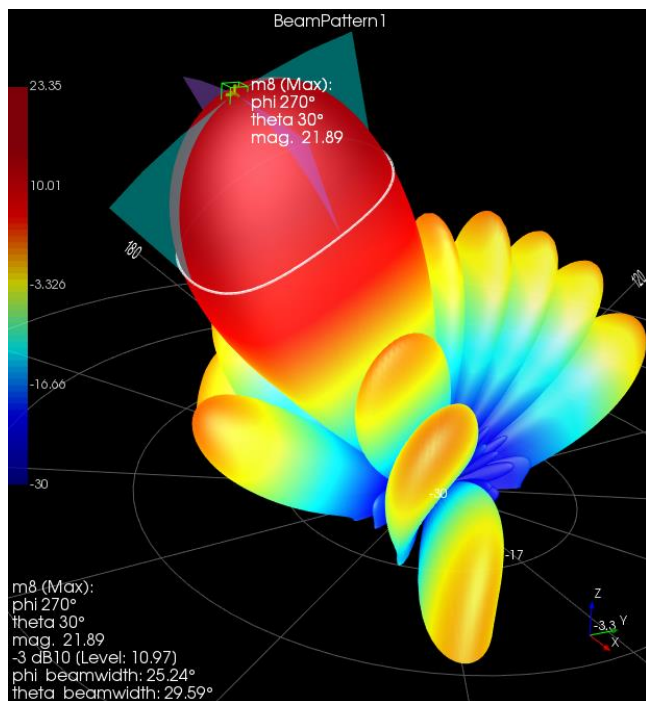


Floating point weights



Gain=4bits, Phase=3bits

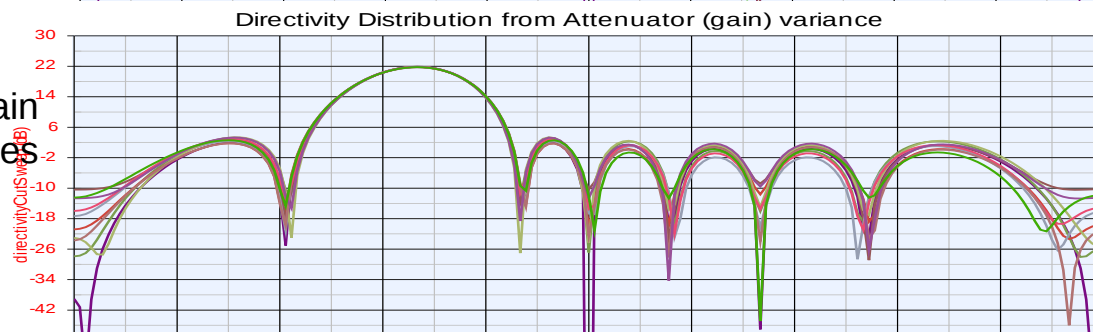
蒙特卡洛分析及阵元失效分析



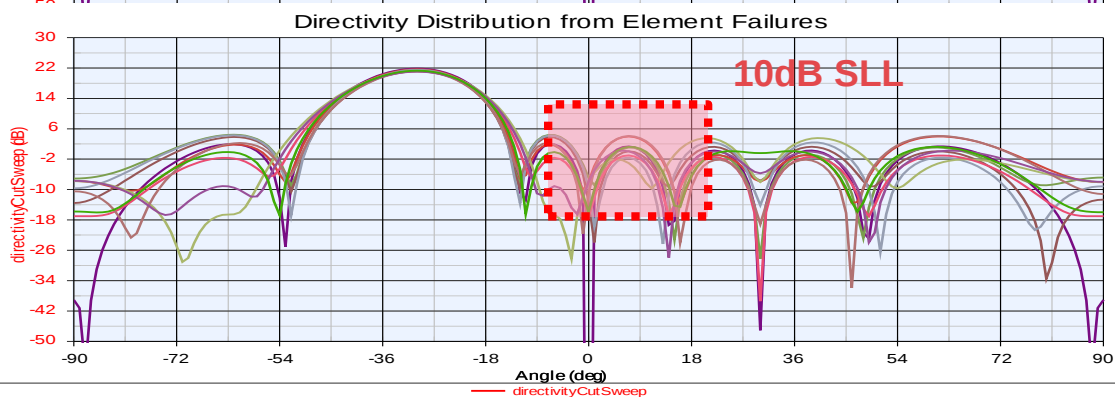
Phase Shift
Variances



Atten/Gain
Variances

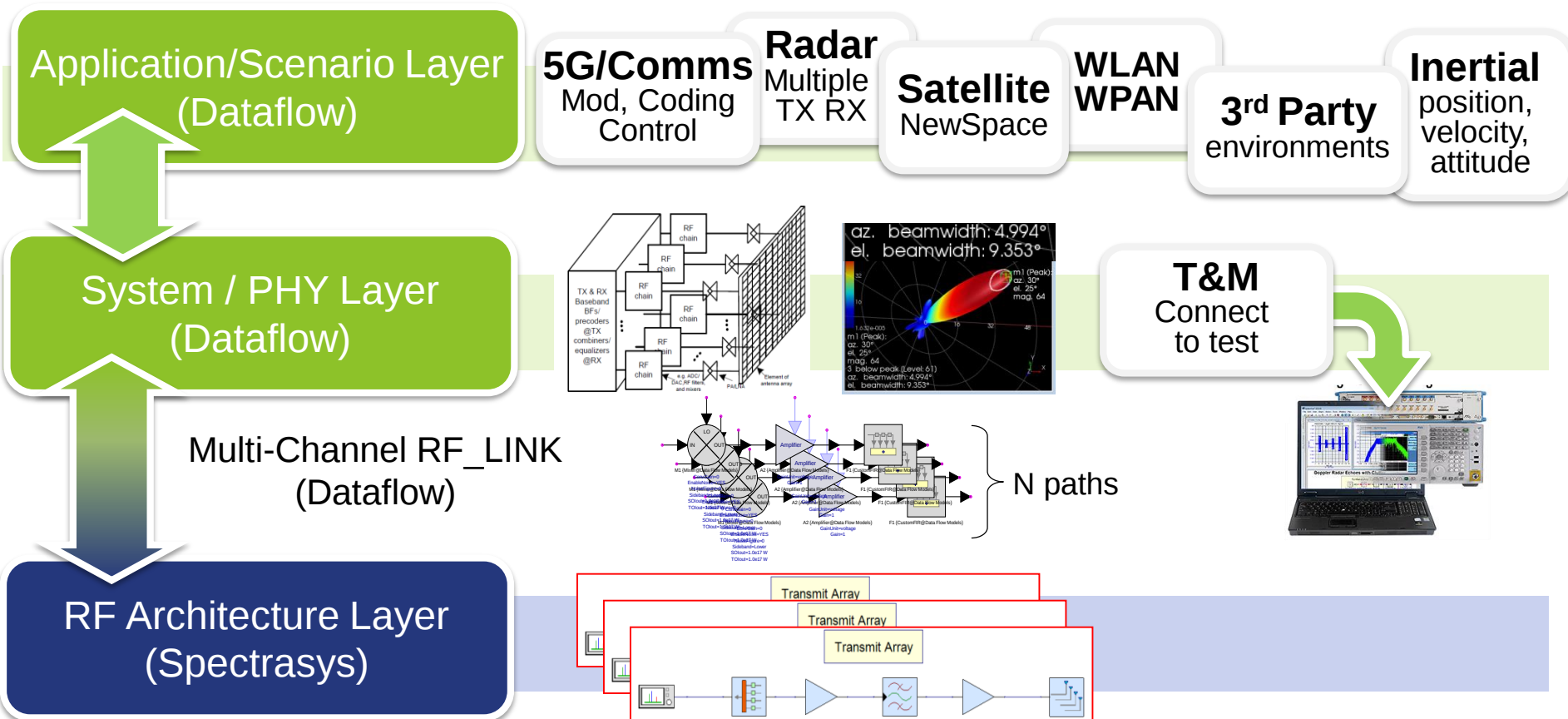


Element
Failures

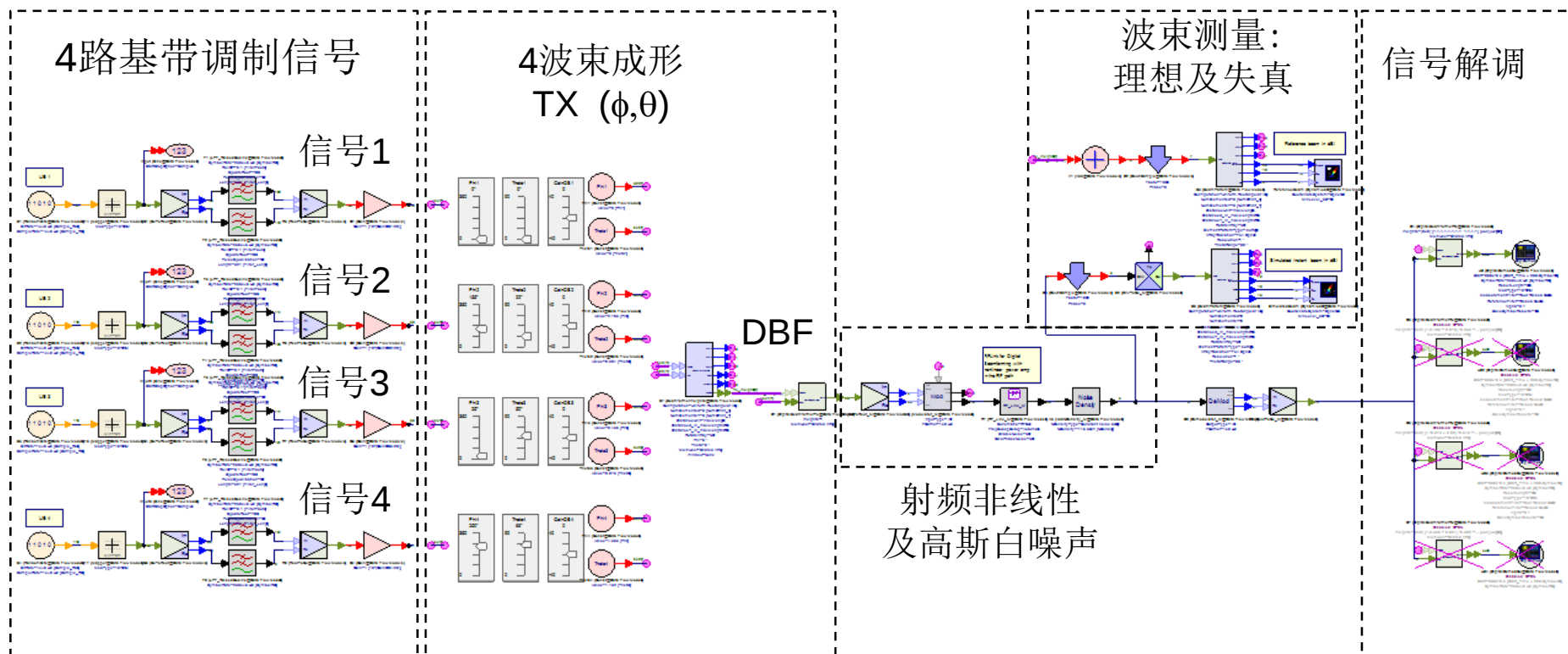


相控阵系统架构设计流程

- A common “cockpit” across multiple disciplines : BB, RF, System, Application, T&M

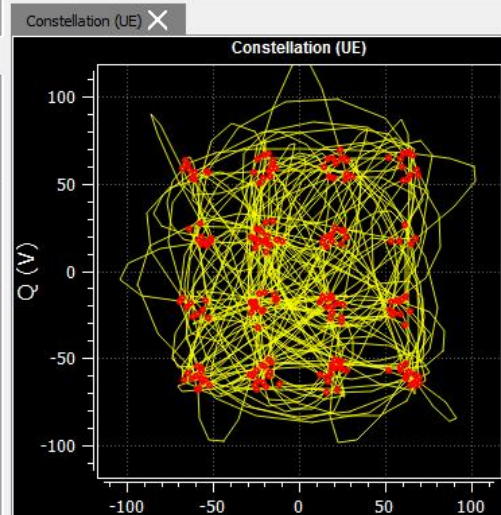
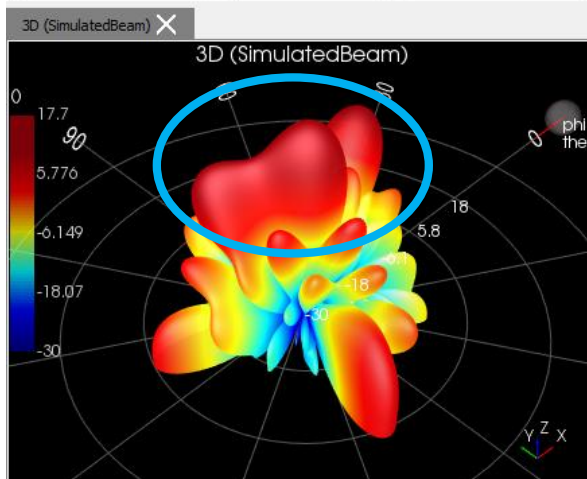
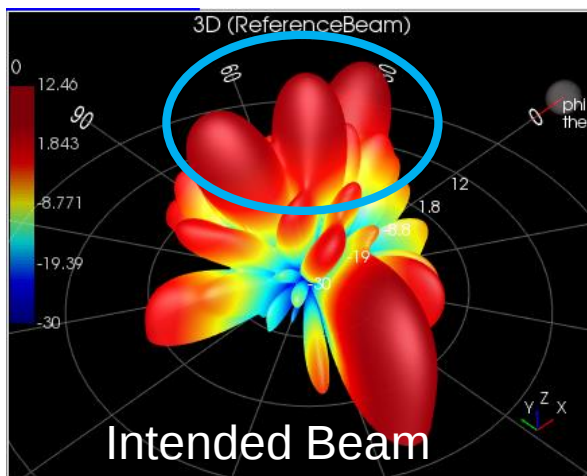


相控阵系统仿真

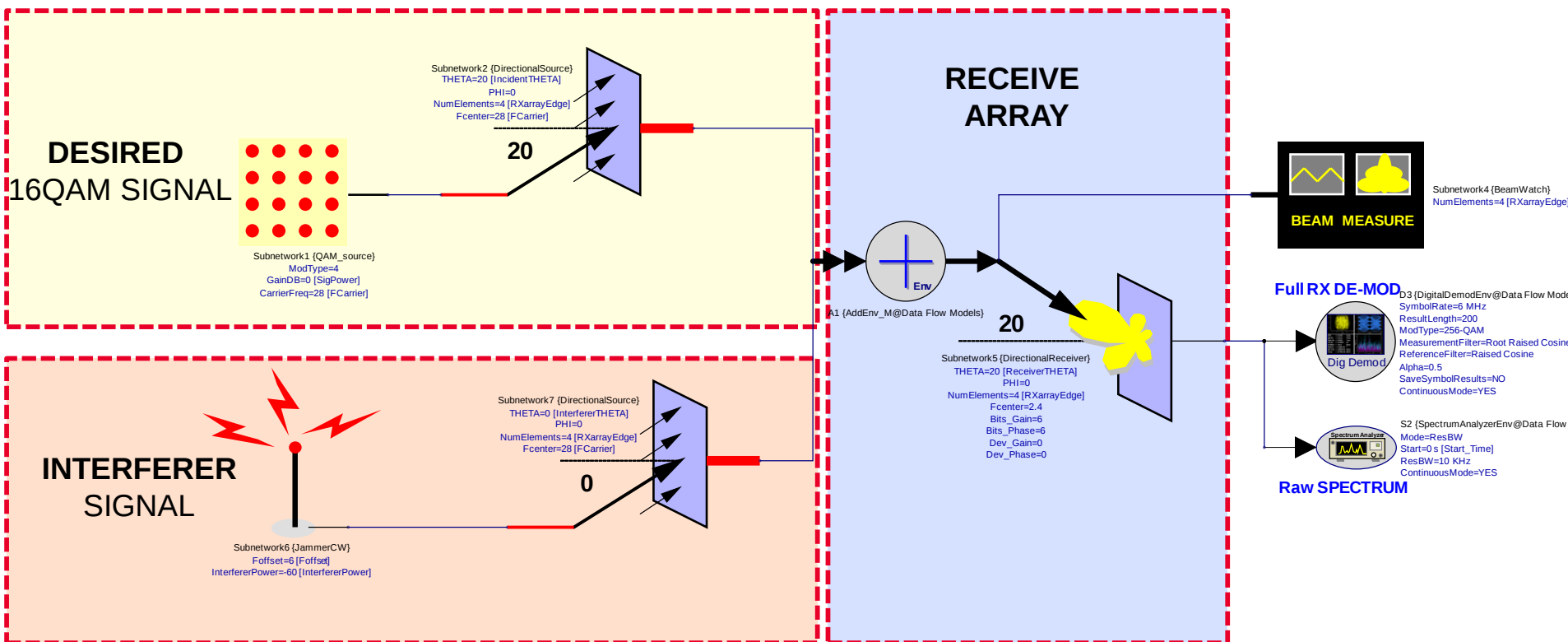


阵列损伤的影响 – Nonlinear Interference from Multiple users

- Large peak from User 1 can compress array TX amplifiers → All signals become distorted
 - AM-AM : sidelobes
 - AM-PM : width, direction
- Able to monitor the dynamic time-varying quality of each of
 - the 4 beams,
 - the 4 signals (EVM, ACLR)

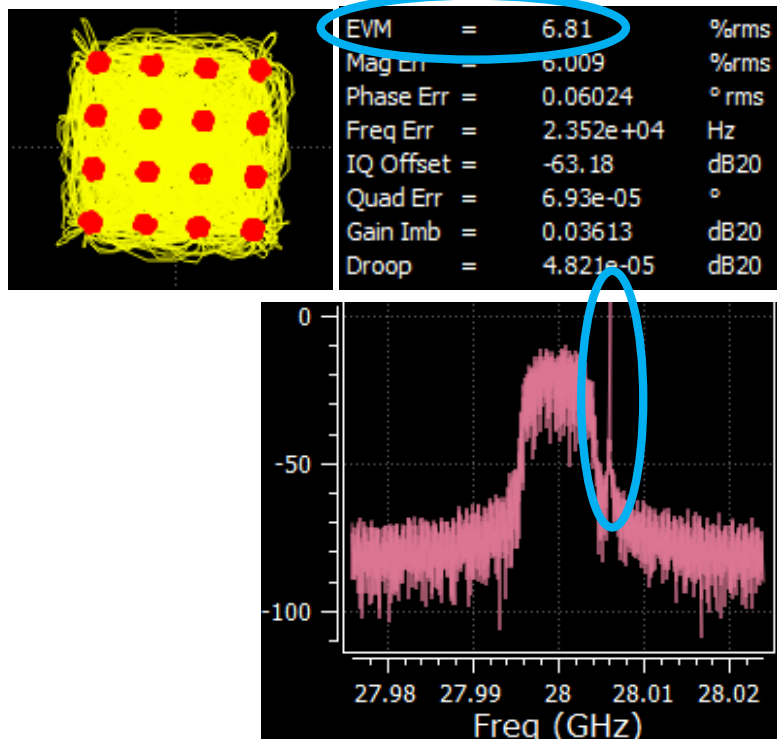


阵列损伤的影响– Nonlinear Interference scenarios



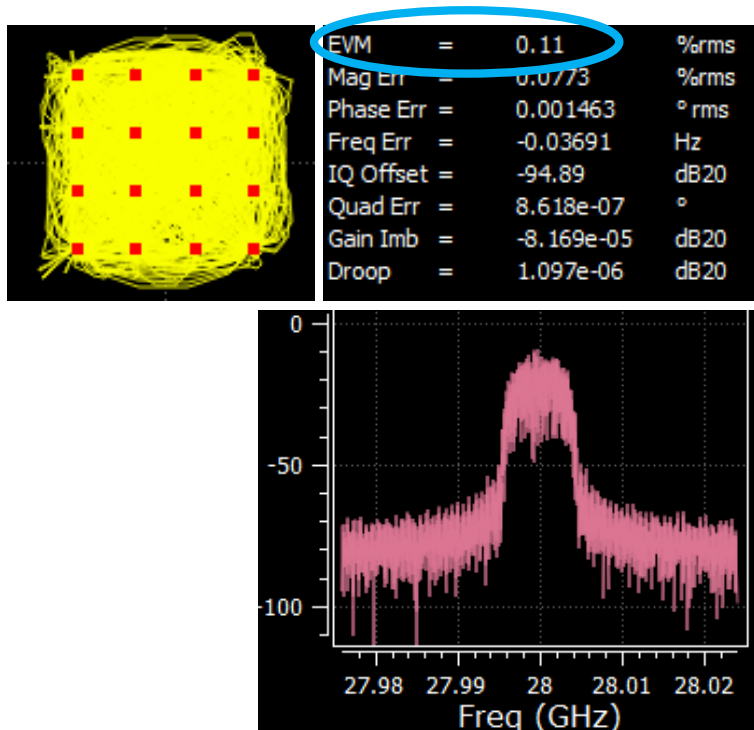
空间干扰信号

- In-band interference, coming from an undesired direction



空间干扰信号

- How many elements/power does it take to get $\text{EVM} < 3\%$

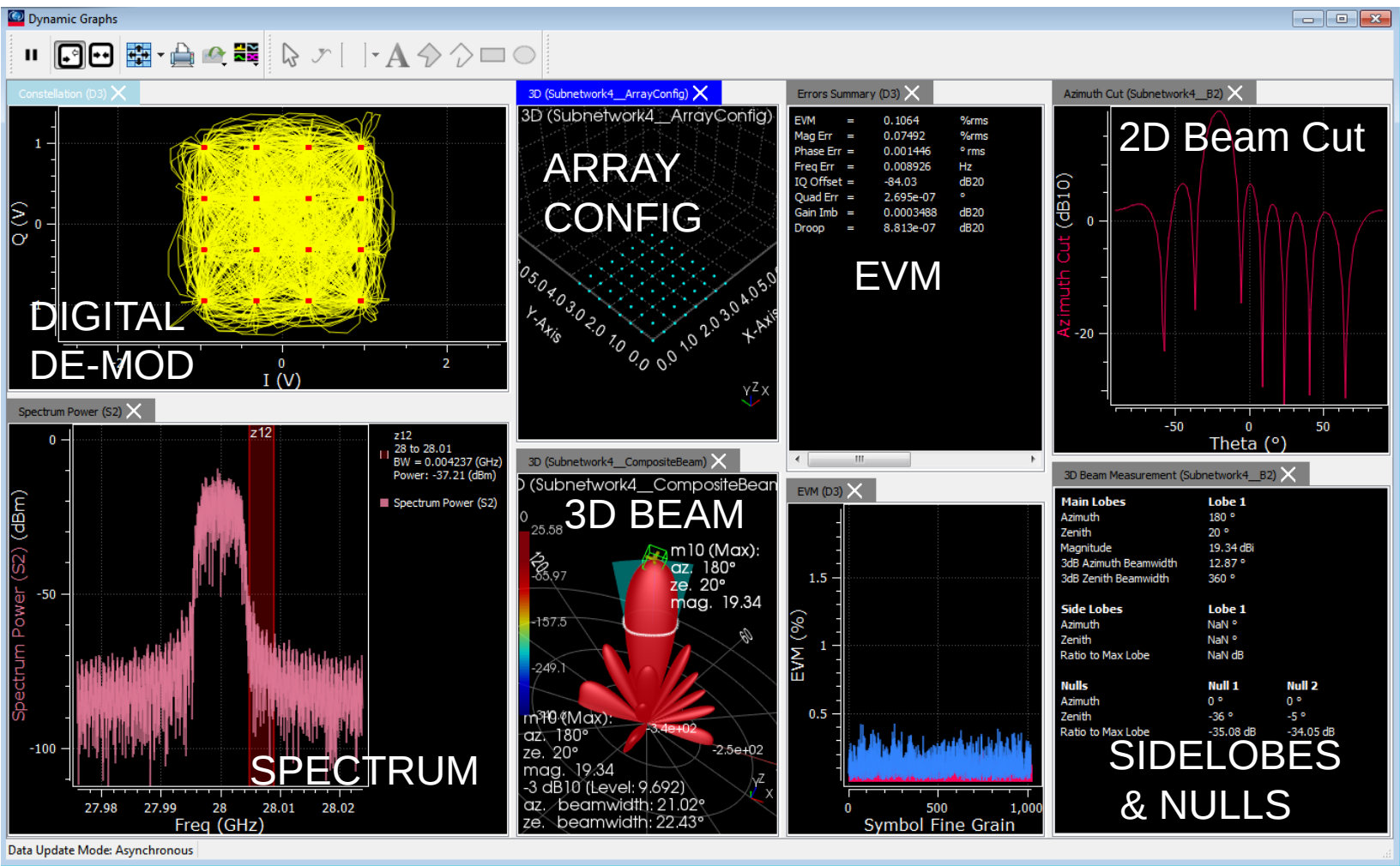


“Yes, I can hear you now, on my 5G phone.”



“Help! Help! I’m being repressed by a beamforming NULL”

测试信号质量，评估ABF/DBF影响

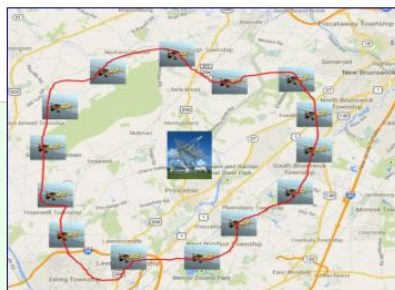


雷达应用 – a “tracking” scenario

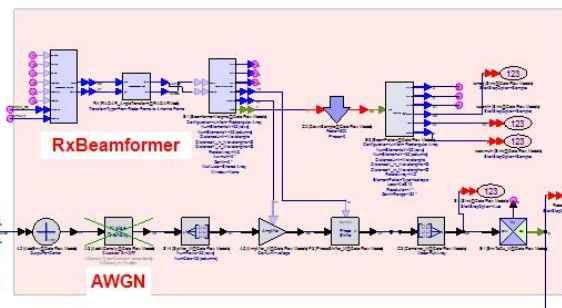
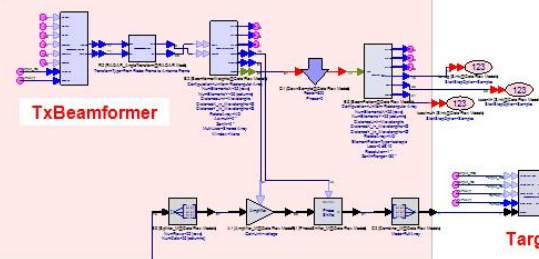
- Beamforming to follow Lat/Long trajectory of aircraft

SystemVue 2016
Pulsed-Doppler AESA Radar Tracking Scenario

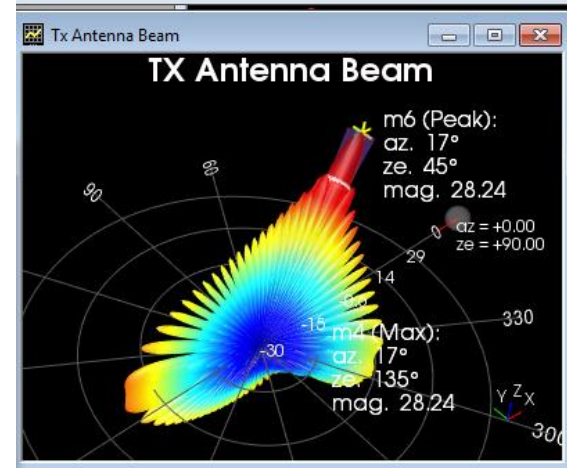
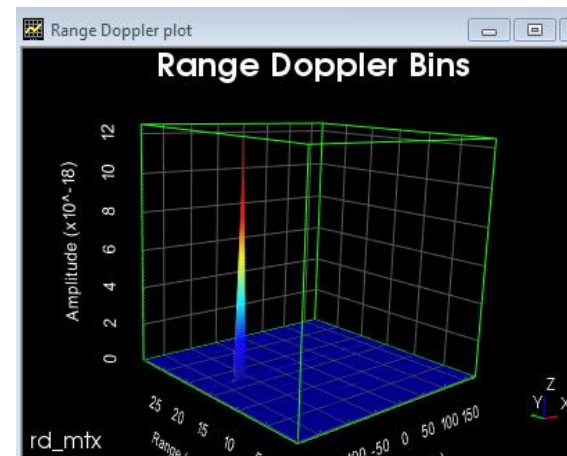
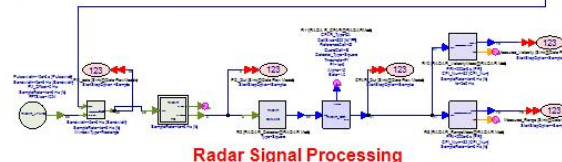
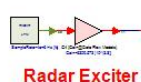
Trajectory Layer



Antenna

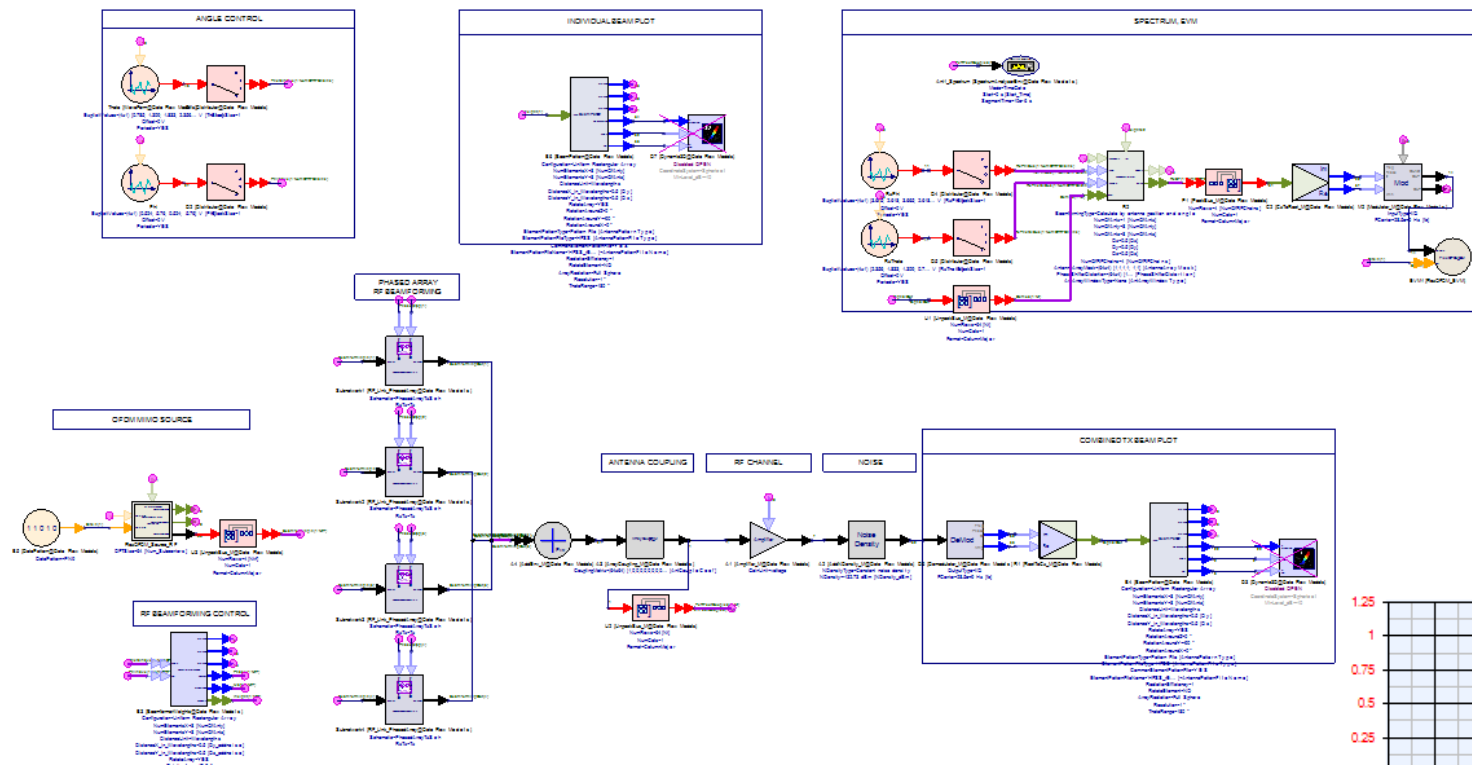


Radar Baseband

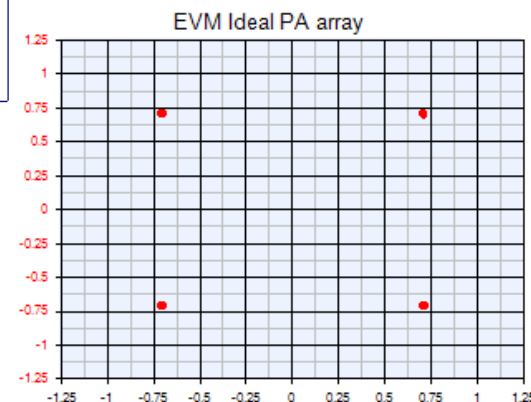


5G 应用: OFDM link, using linear TX beamformer

- 4-layer MIMO signal, 2 GHz bandwidth at 28.5GHz carrier

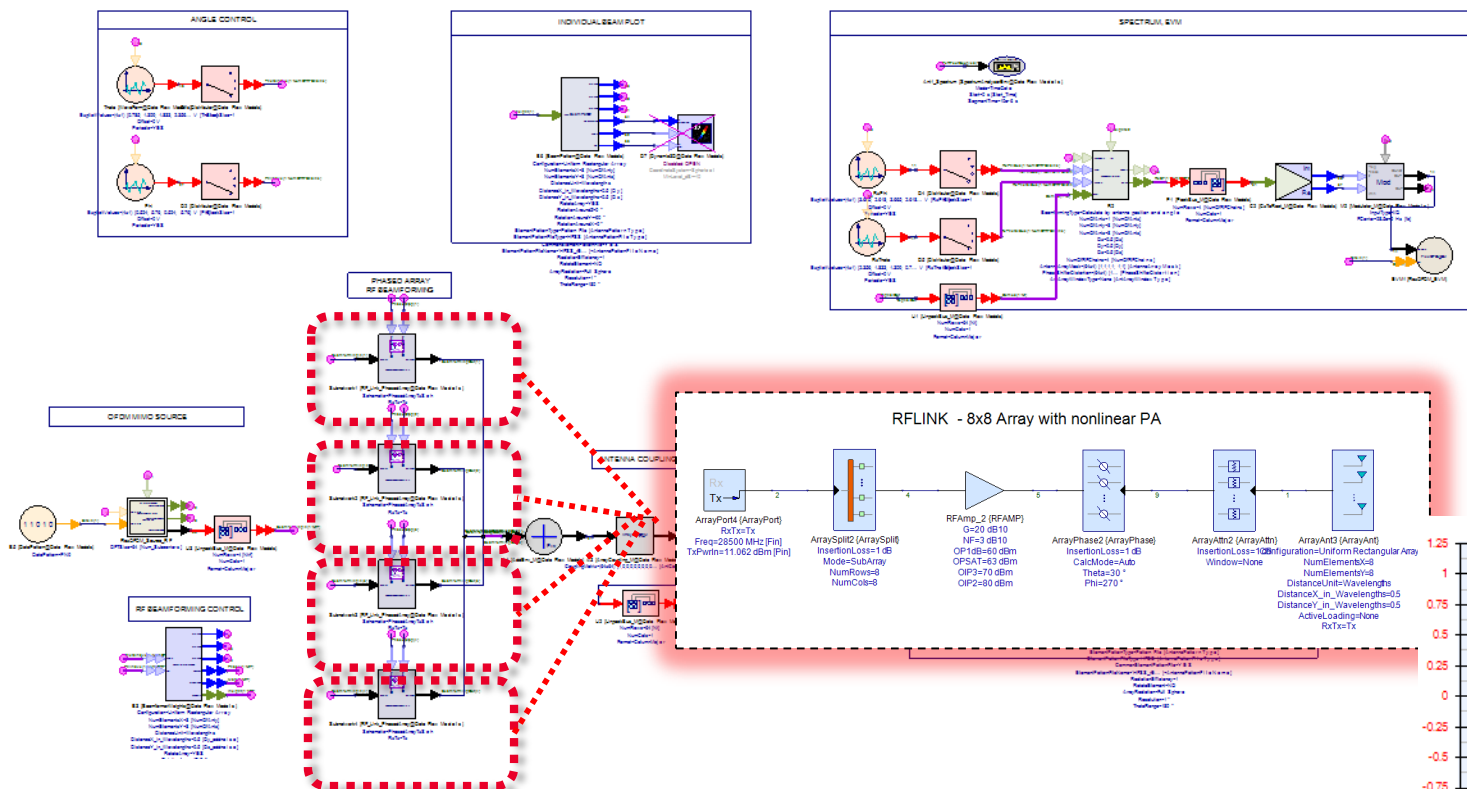


EVM Ideal Array
-55.115



5G 应用: OFDM link, using nonlinear TX beamformer (RF_Link)

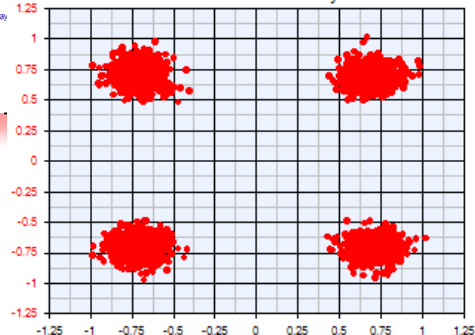
- Power-handling limitations creating system-level effects



EVM Nonlinear Array

-18.87

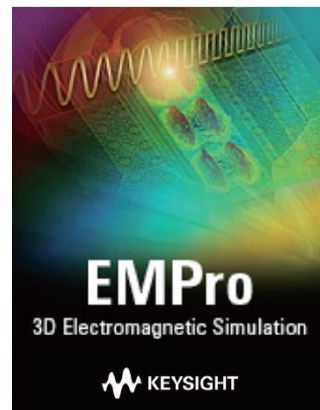
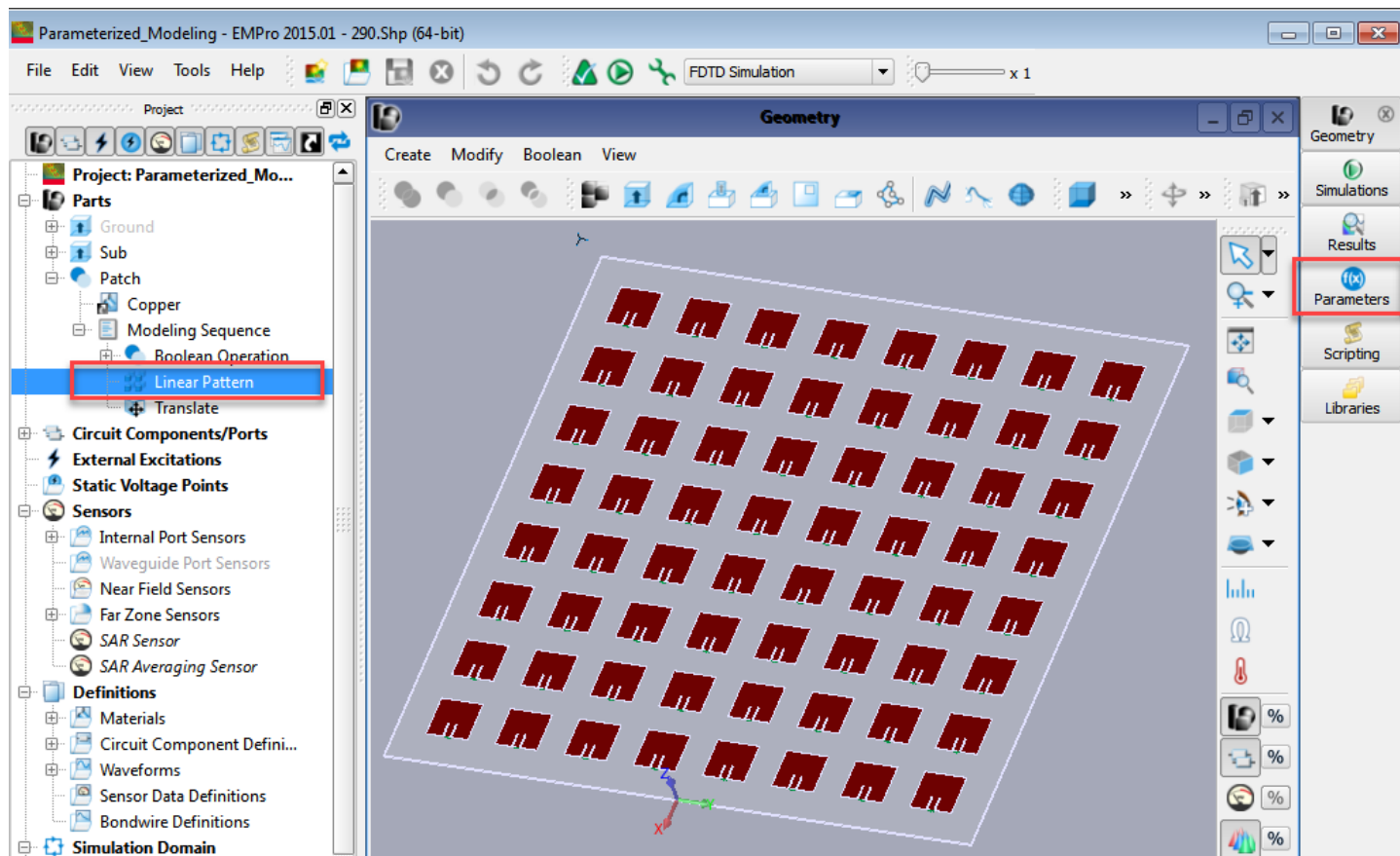
EVM Nonlinear PA array



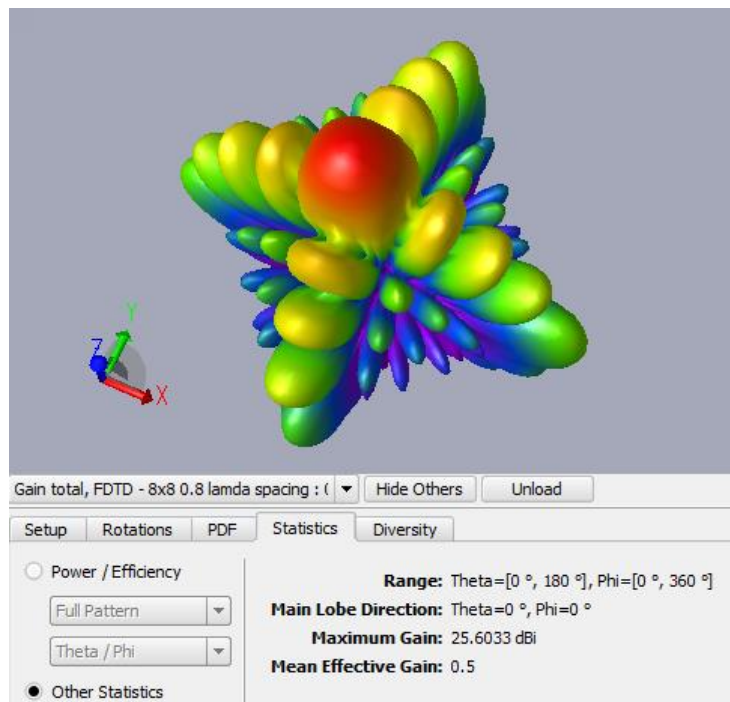
内容安排

- 相控阵系统设计面临的挑战
- 相控阵系统设计分析
- 相控阵单元电路设计
- 总结

相控阵天线设计仿真-- EMPro参数化建模

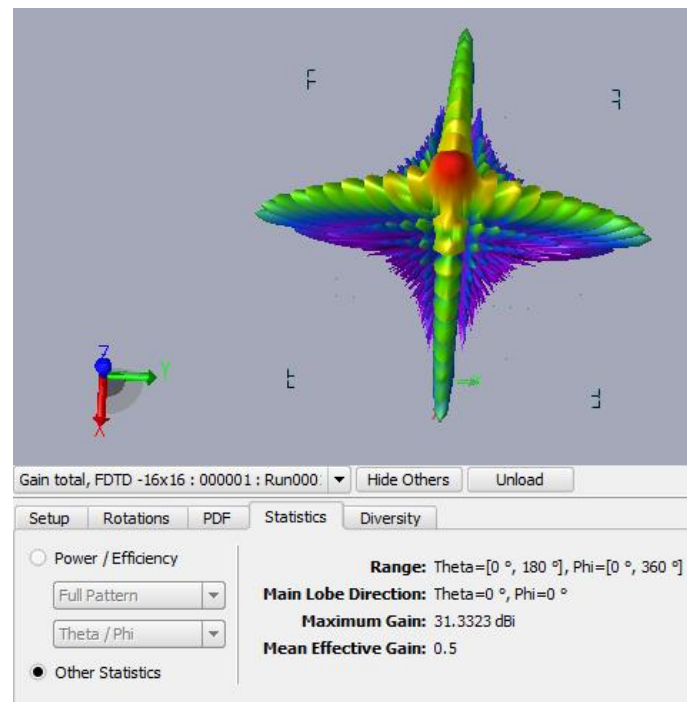


EMPro阵列天线设计仿真 (FDTD)



8*8 (0.8 lamda spacing)

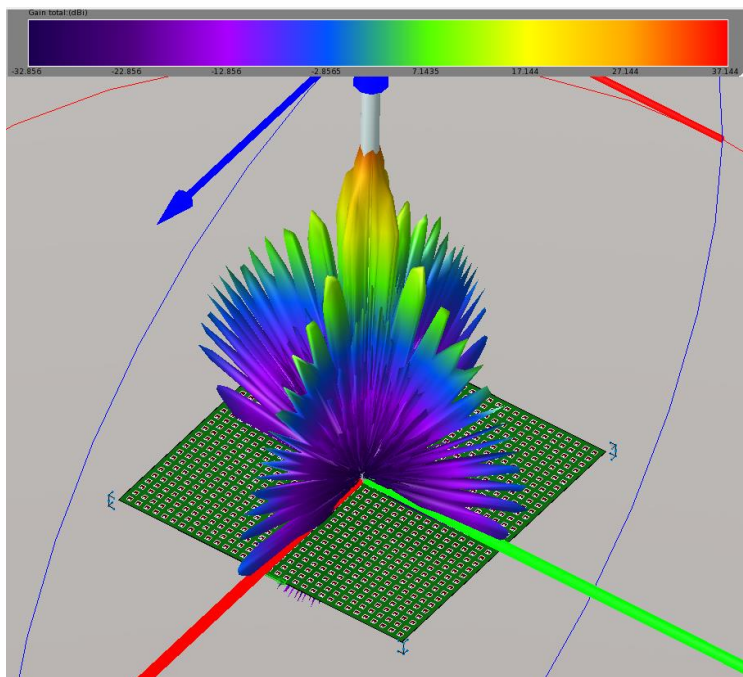
4块K80 GPU加速卡
4min, 40s



16*16

4块K80 GPU加速卡
27min, 46s

EMPro阵列天线设计仿真(FDTD)



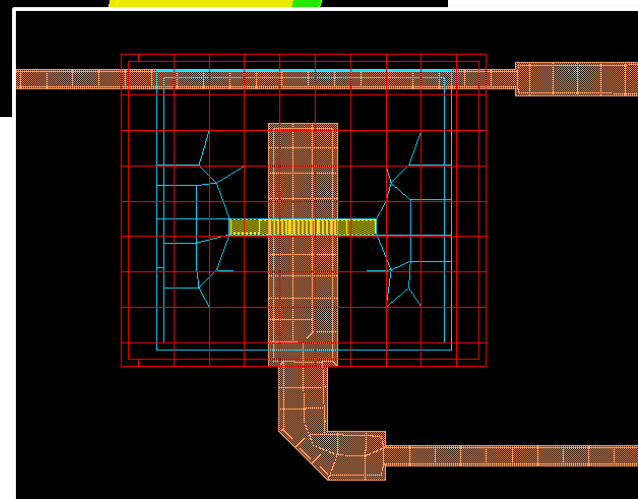
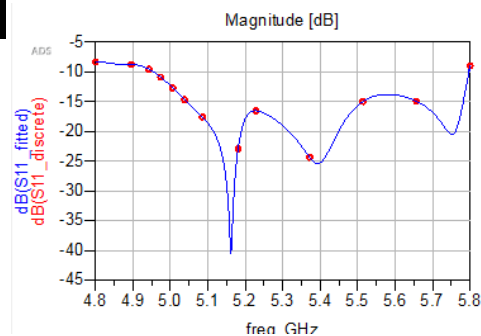
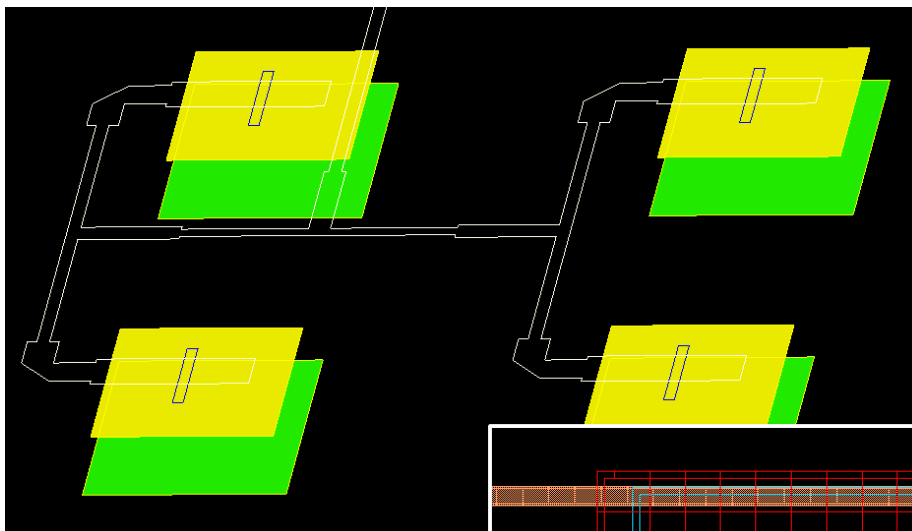
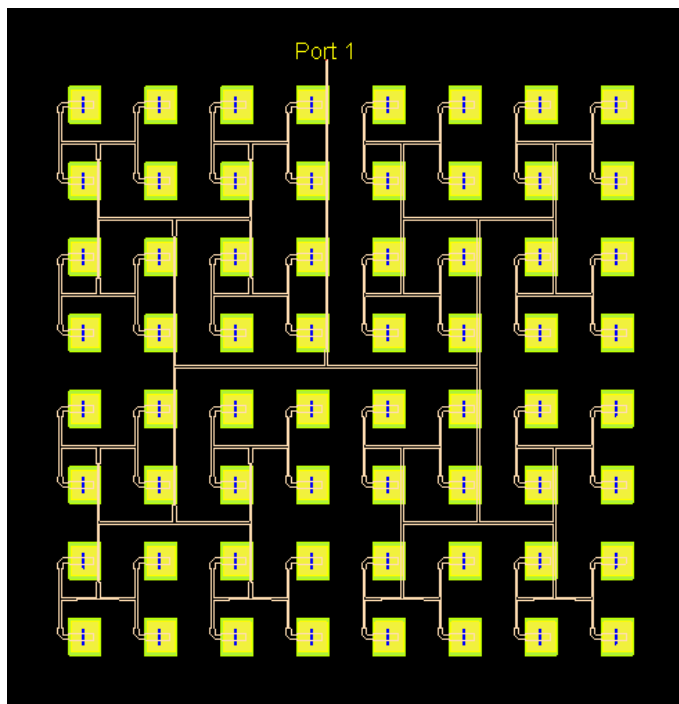
使用FDTD对32*32阵列仿真
使用4块K80 GPU加速卡

```
48.06% 24030 / 50000 -29.89 / -30.00 2hrs, 25m, 46s / 2hrs, 37m, 32s
48.08% 24040 / 50000 -29.89 / -30.00 2hrs, 25m, 48s / 2hrs, 37m, 26s
48.10% 24050 / 50000 -29.89 / -30.00 2hrs, 25m, 50s / 2hrs, 37m, 21s
48.12% 24060 / 50000 -29.89 / -30.00 2hrs, 25m, 52s / 2hrs, 37m, 15s
48.14% 24070 / 50000 -29.89 / -30.00 2hrs, 25m, 55s / 2hrs, 37m, 11s
48.16% 24080 / 50000 -29.89 / -30.00 2hrs, 25m, 57s / 2hrs, 37m, 6s
48.18% 24090 / 50000 -29.89 / -30.00 2hrs, 25m, 59s / 2hrs, 37m
48.20% 24100 / 50000 -29.89 / -30.00 2hrs, 26m, 1s / 2hrs, 36m, 55s

Saving steady state fields for far zone computations.
Time step 24100, -30.18 dB convergence reached. Computing last time step.
Executing simulation with 8 threads (for supported features).
time step 24100, -30.18 dB convergence reached. Performing post processing.
```

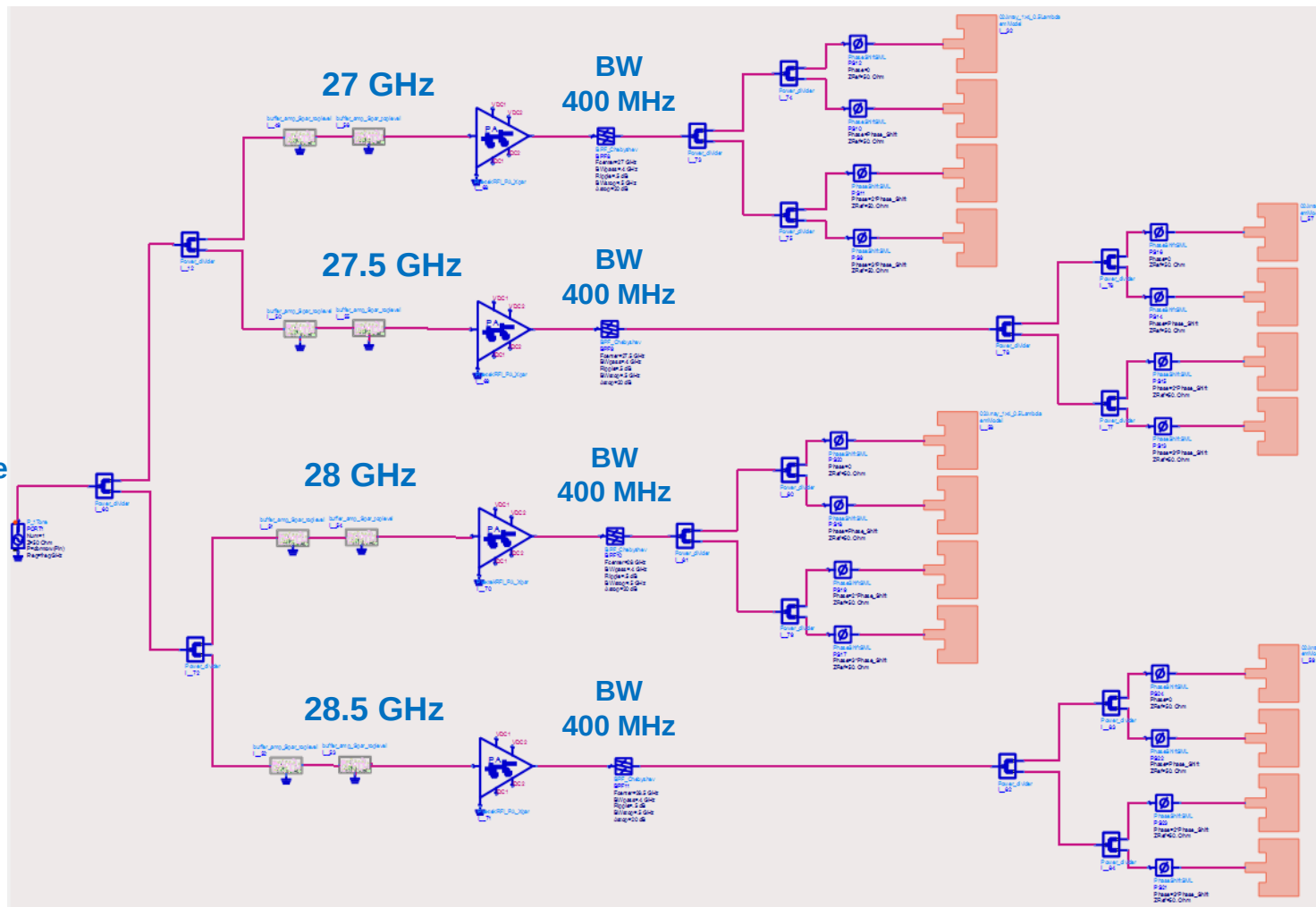
平面天线设计: ADS Momentum 8x8 patch array

Direct EM solution, with weighted signal excitation in post-processor



四通道发射机射频子系统

Power source
Sweep
27 GHz
28.5 GHz
.5 GHz steps



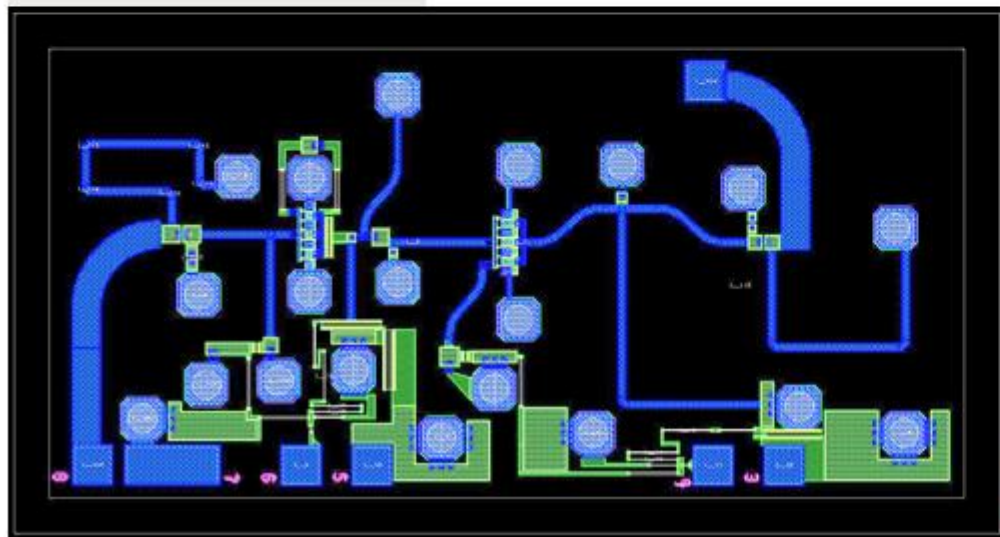
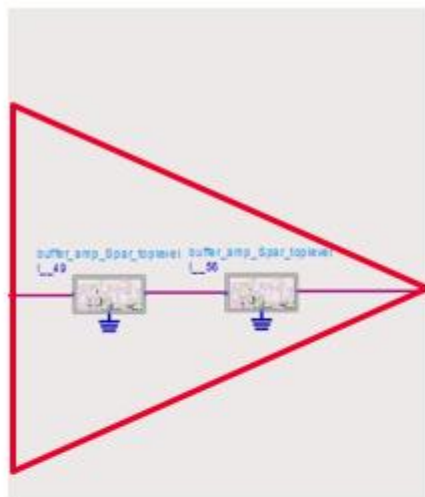
Channel 1

Channel 2

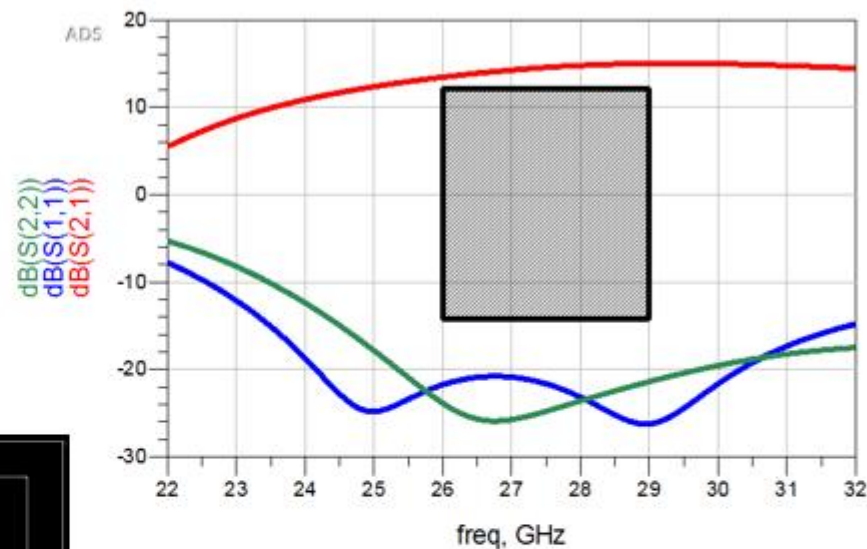
Channel 3

Channel 4

毫米波电路设计仿真



28 GHz Buffer Amplifier



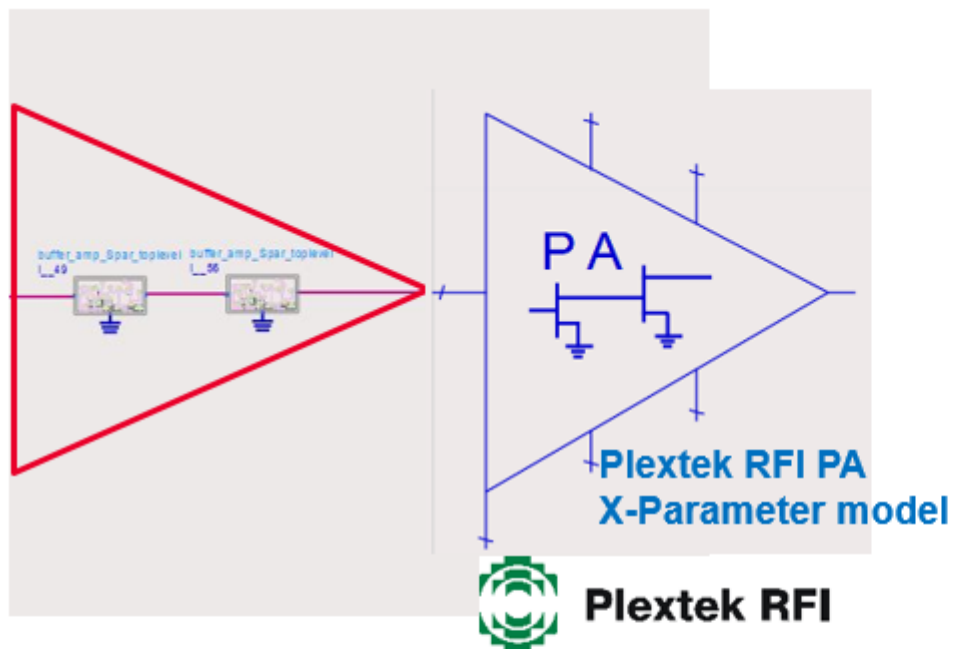
mm-Wave small signal Amp

TriQuint PHEMT process

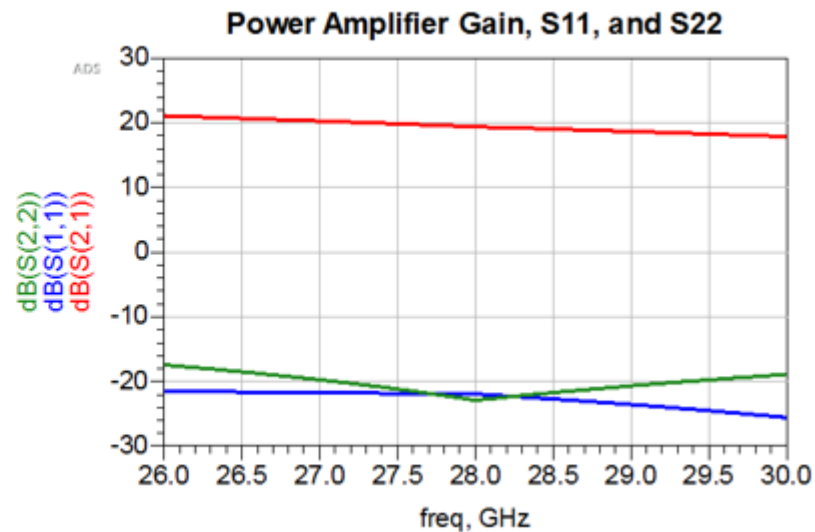
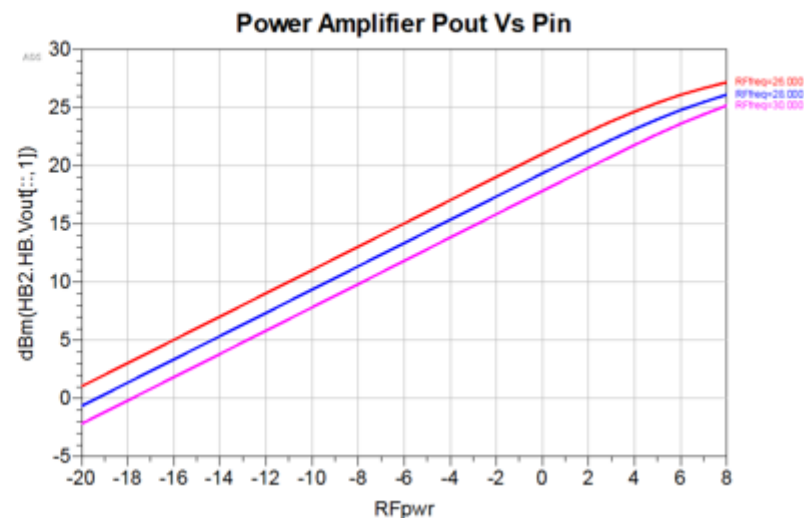


Plextek RFI

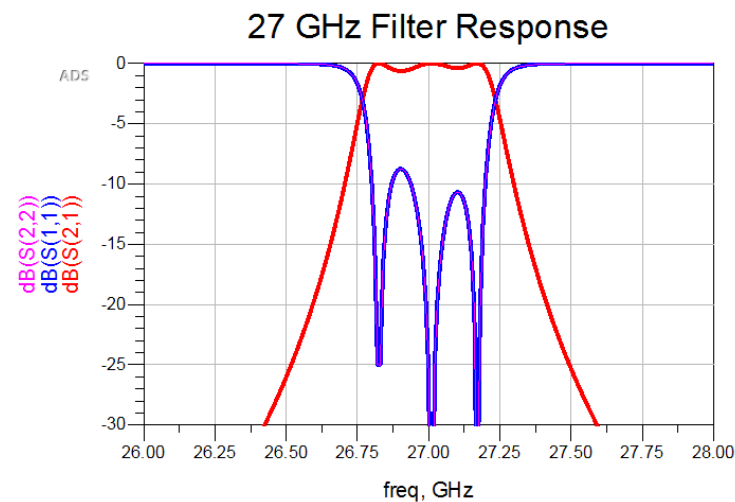
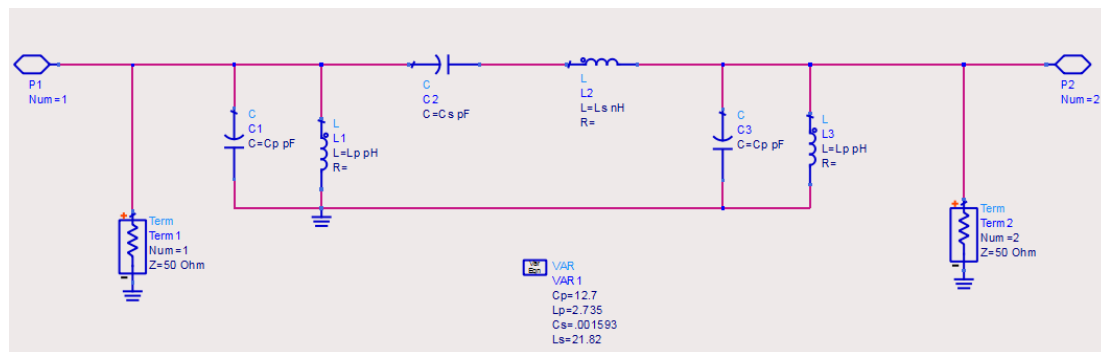
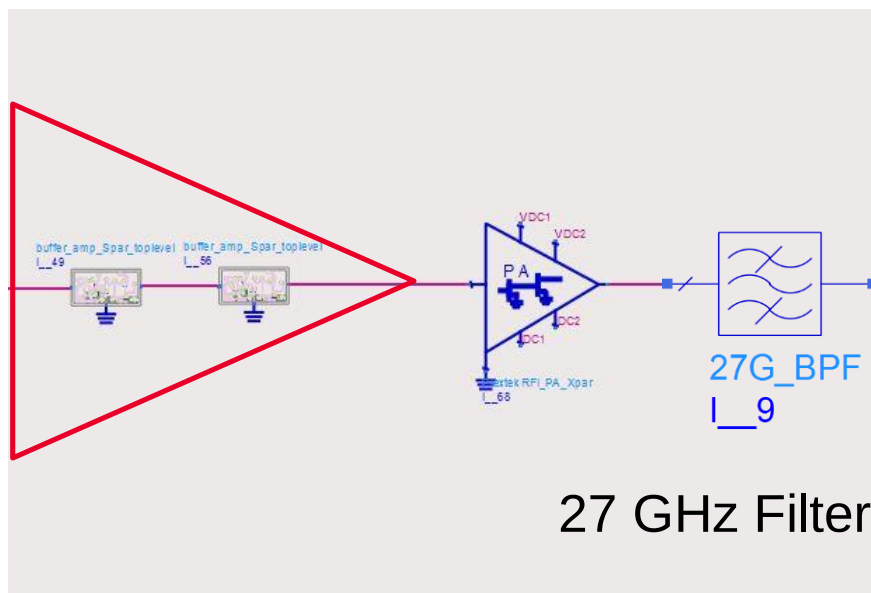
射频子系统级联仿真分析



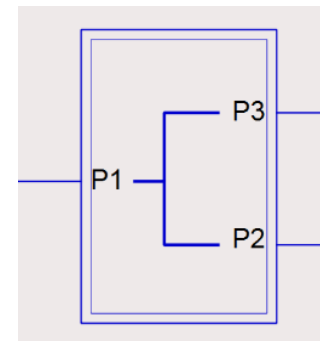
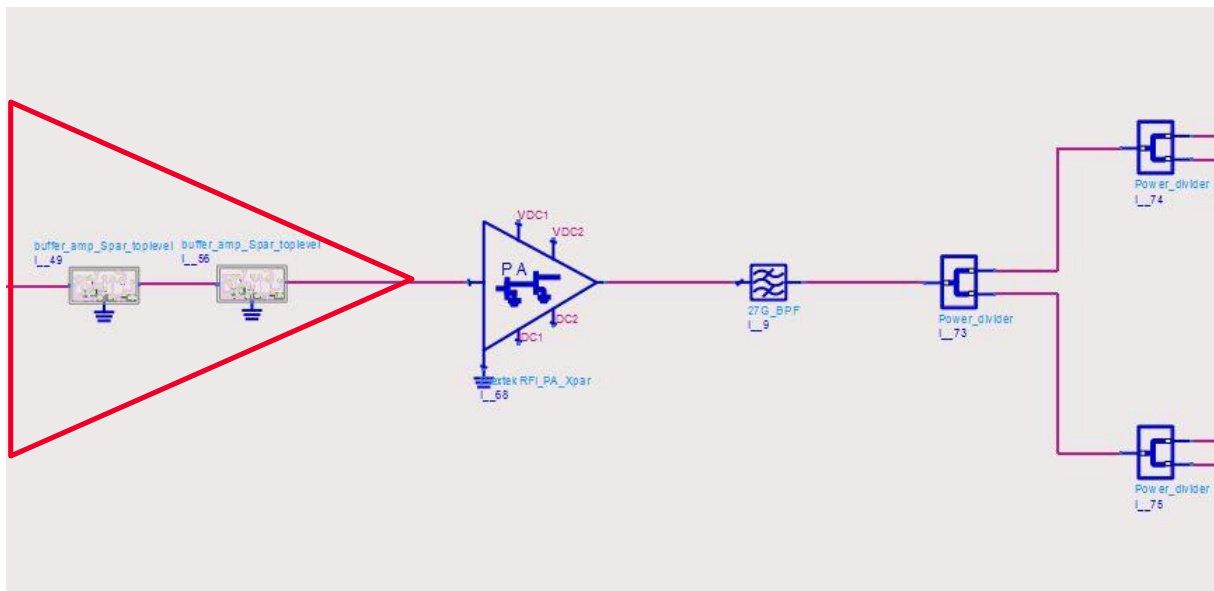
mm-Wave PA
GCS InPDHBT process



射频子系统级联仿真分析

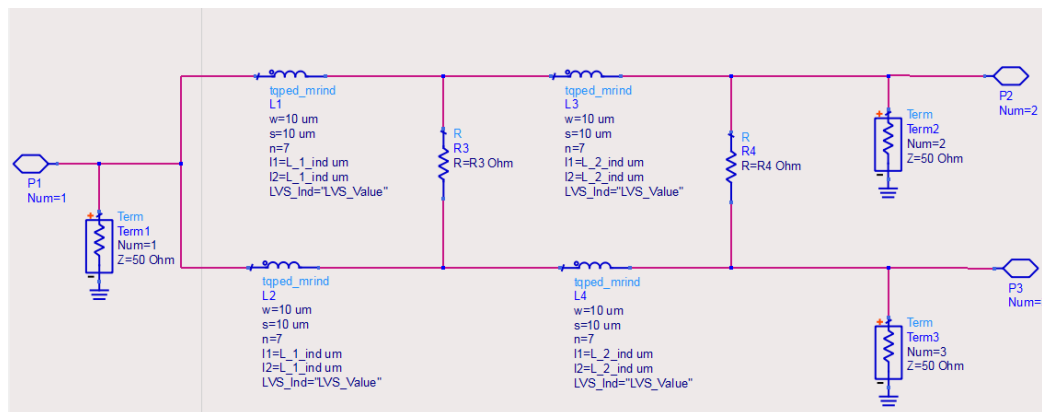
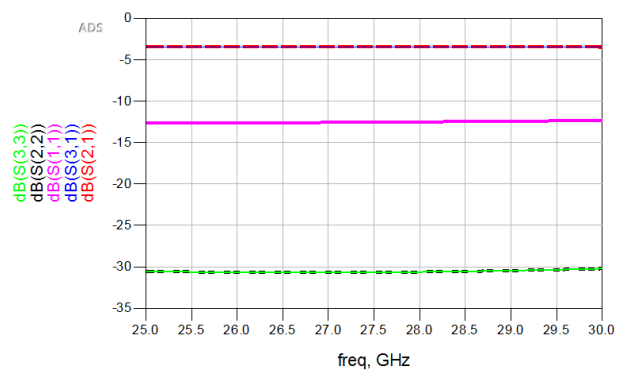


功分器

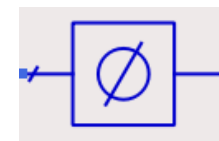
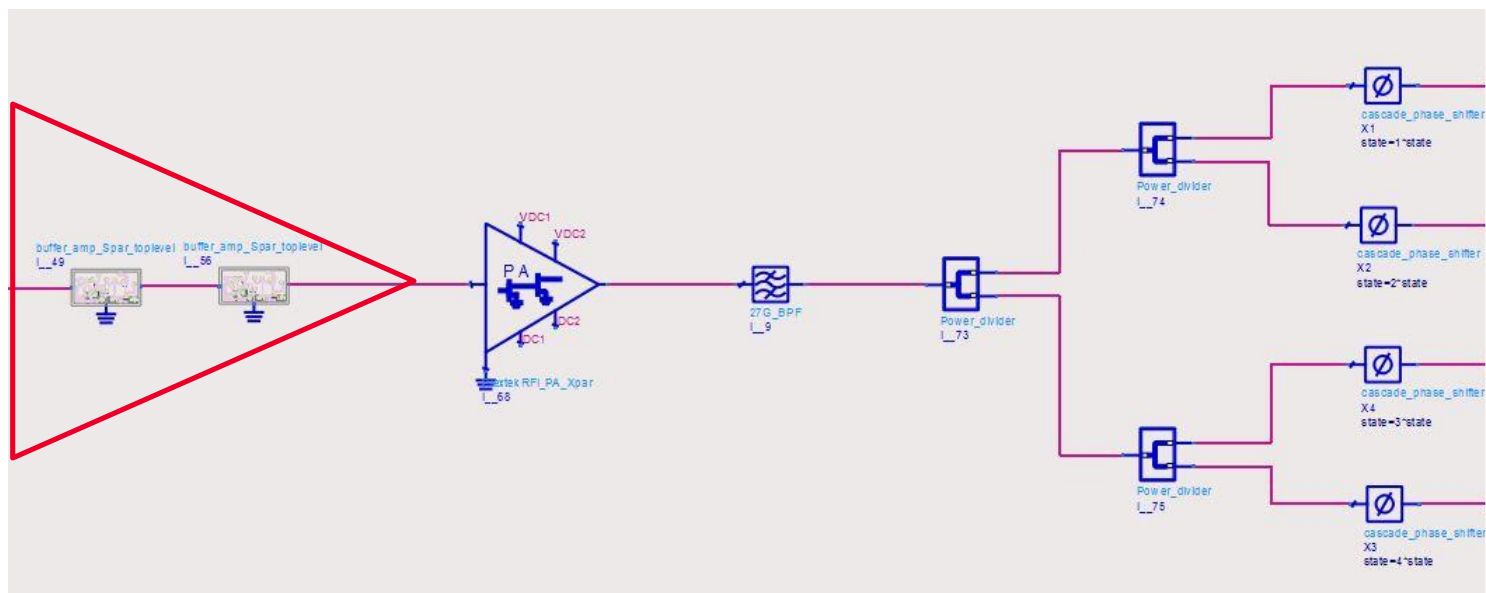


Power Divider
TriQuint Process

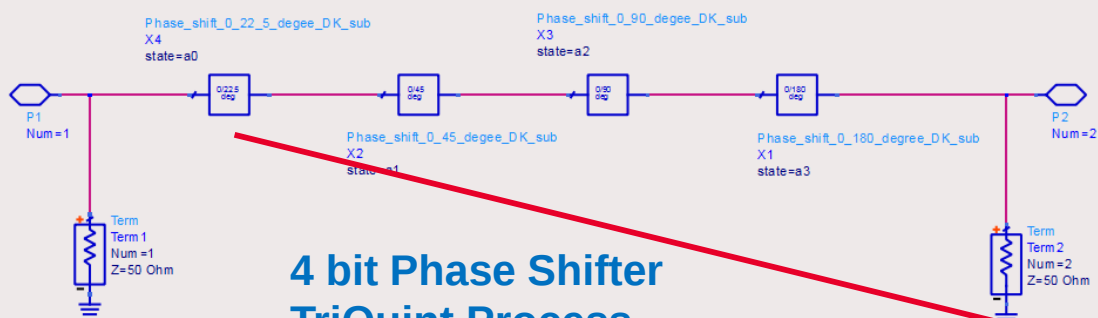
Power Divider S-Parameters



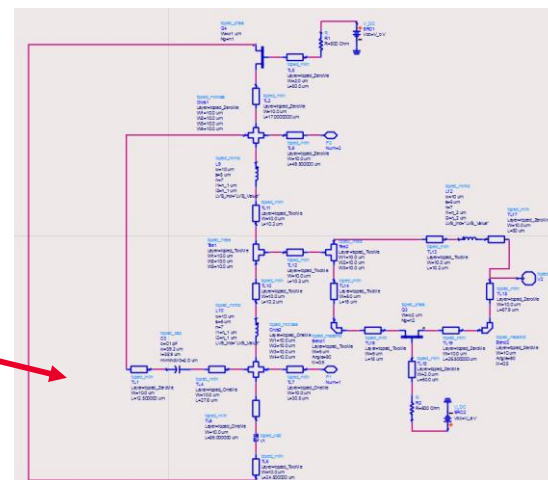
4 位移相器



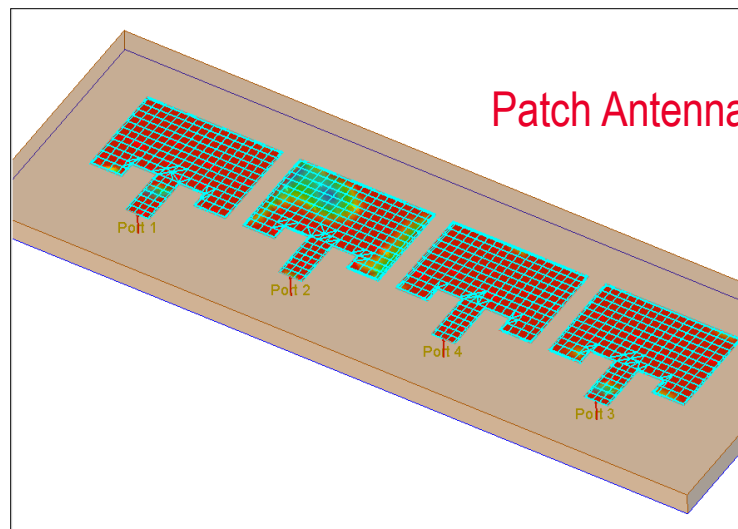
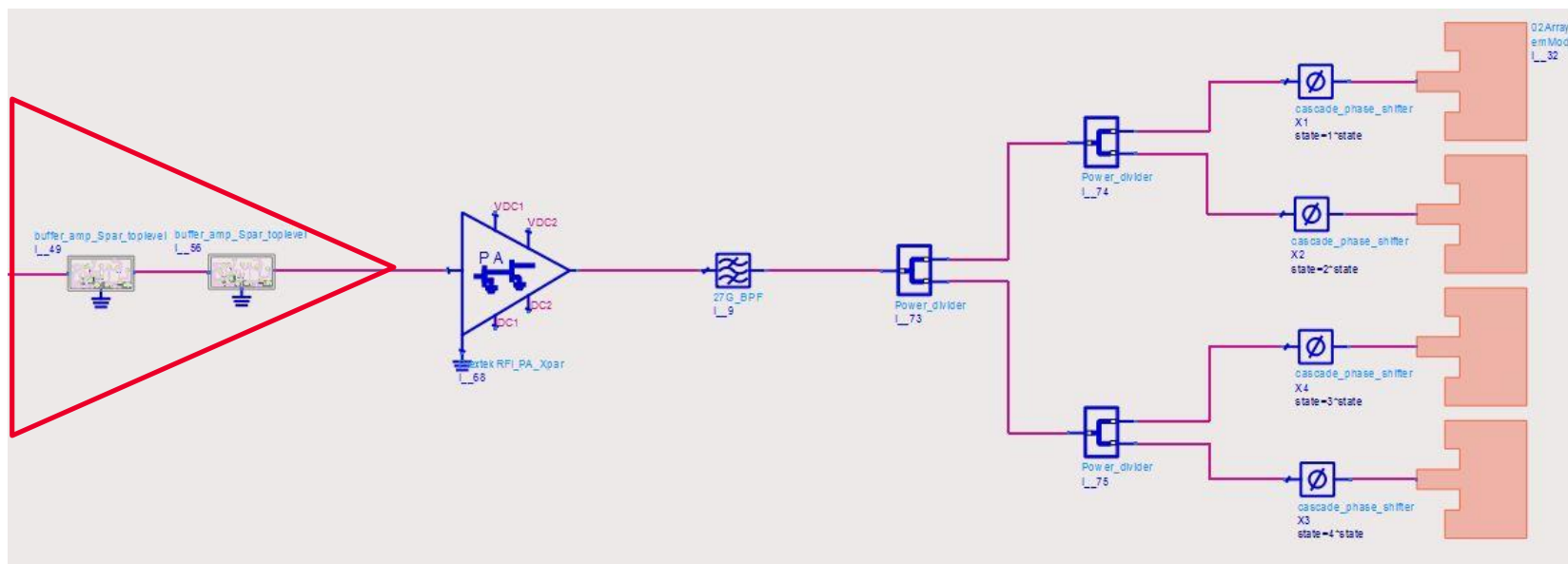
4 bit (16 States) Phase Shifter



4 bit Phase Shifter
TriQuint Process

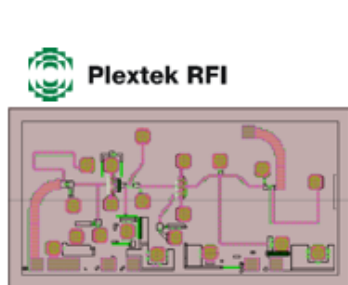


贴片天线 (1X4 Array – $\frac{1}{2}$ Lambda)

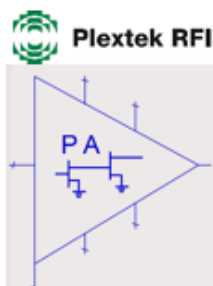


Patch Antenna Design (1X4 array – $\frac{1}{2}$ Lambda)

单通道发射机子系统



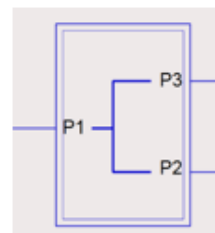
Plextek RFI Buffer Amp



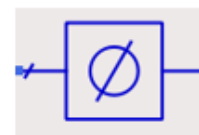
Plextek RFI PA



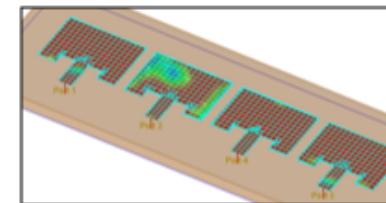
27 GHz BPF



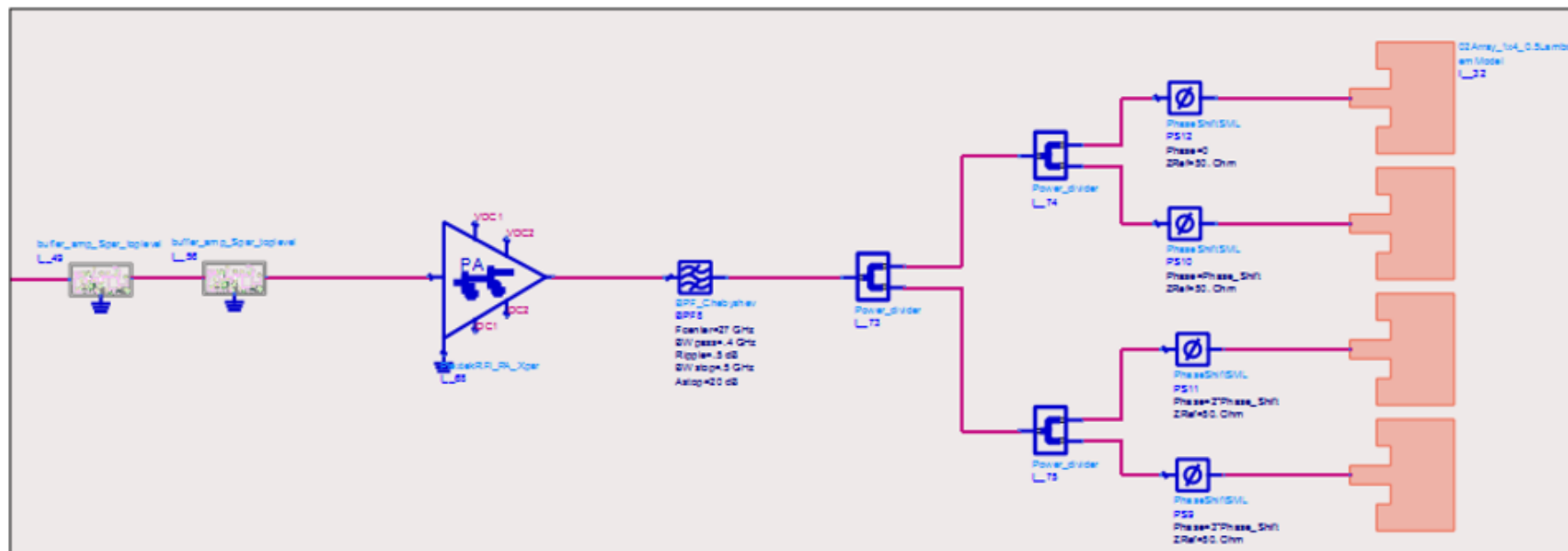
Power Divider



Phase Shifter

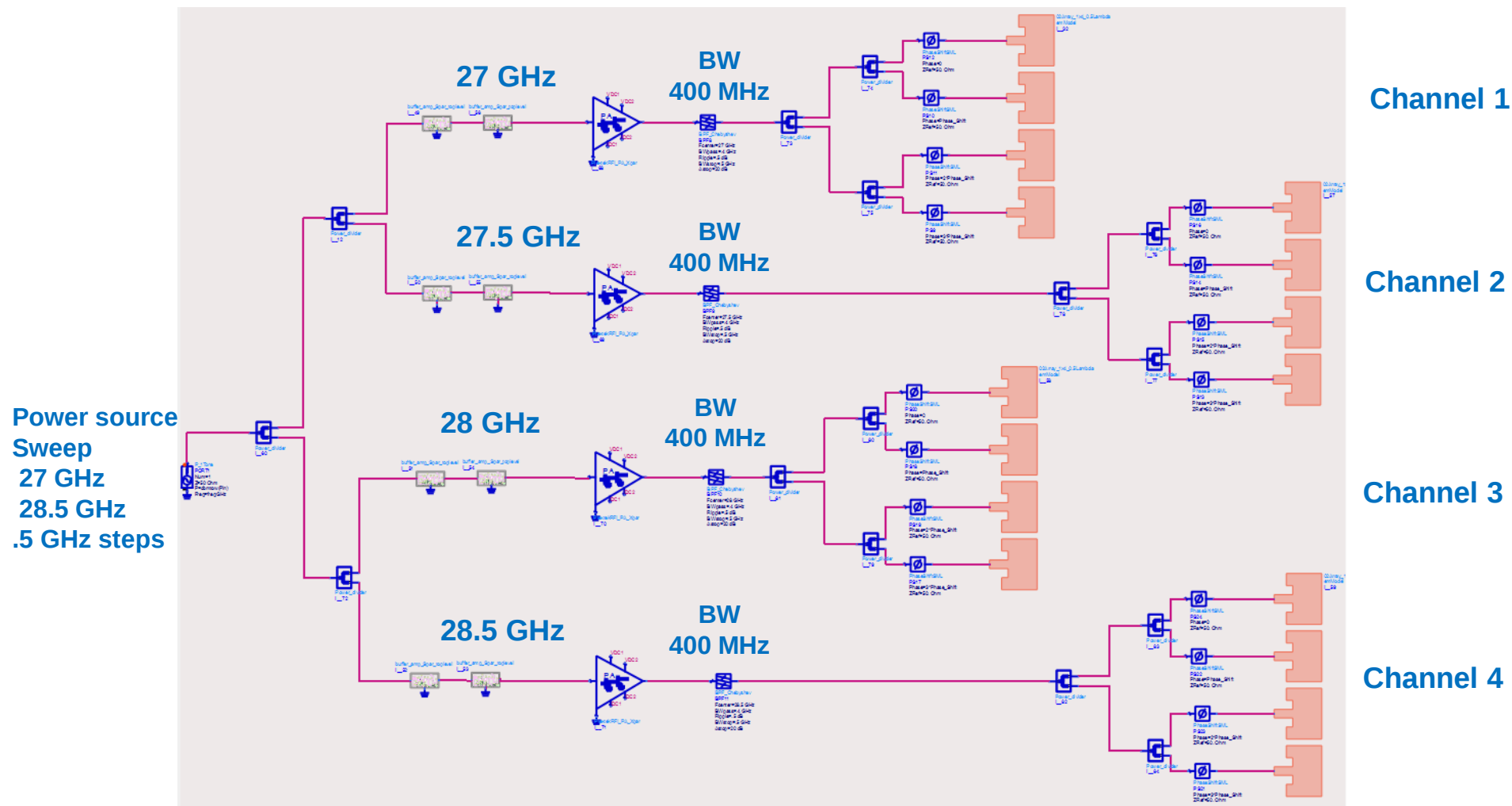


1X4 Array .5 Lambda Patch Antenna



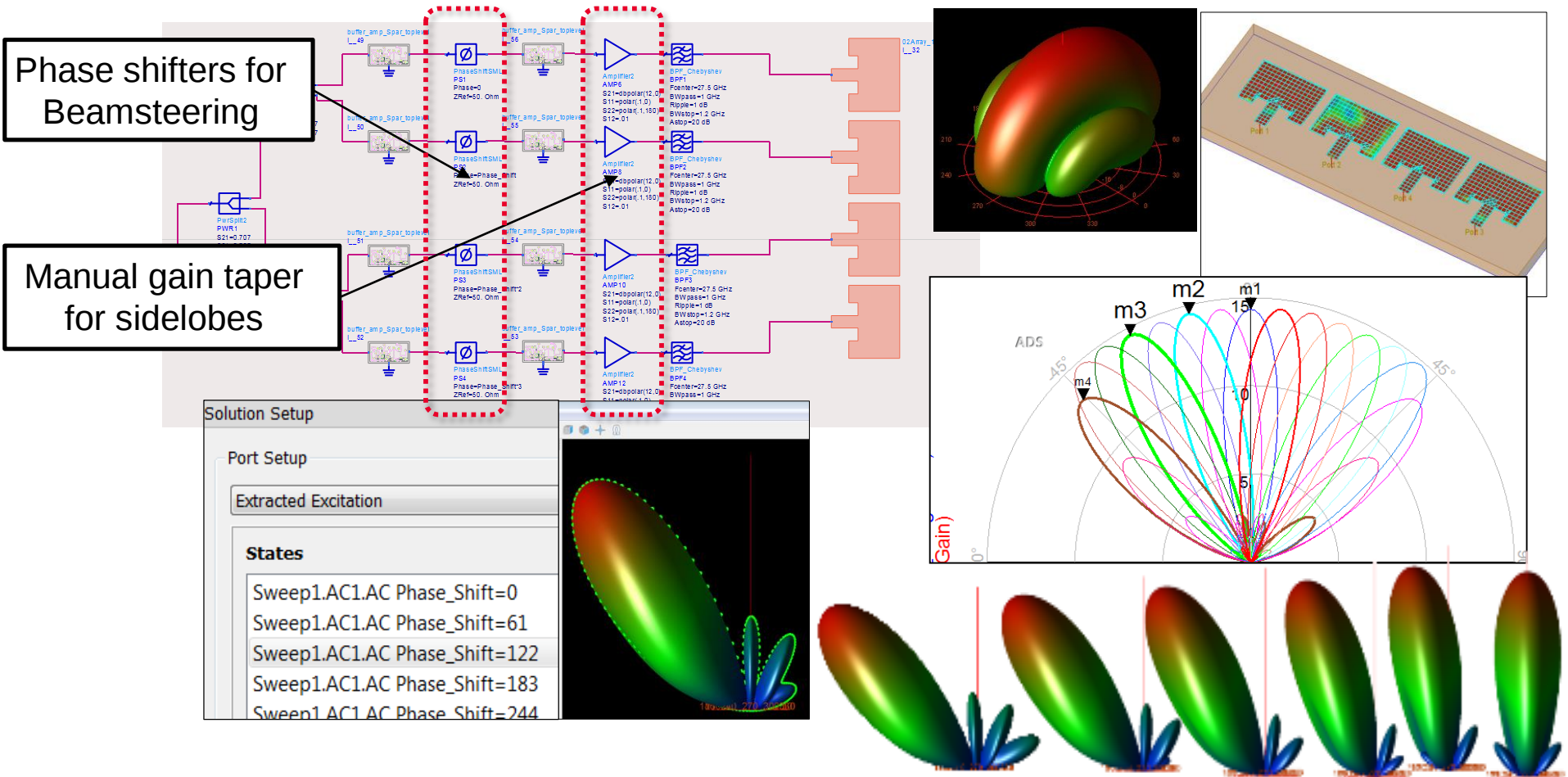
四通道发射机

平面天线/射频子系统/电路/电磁场仿真

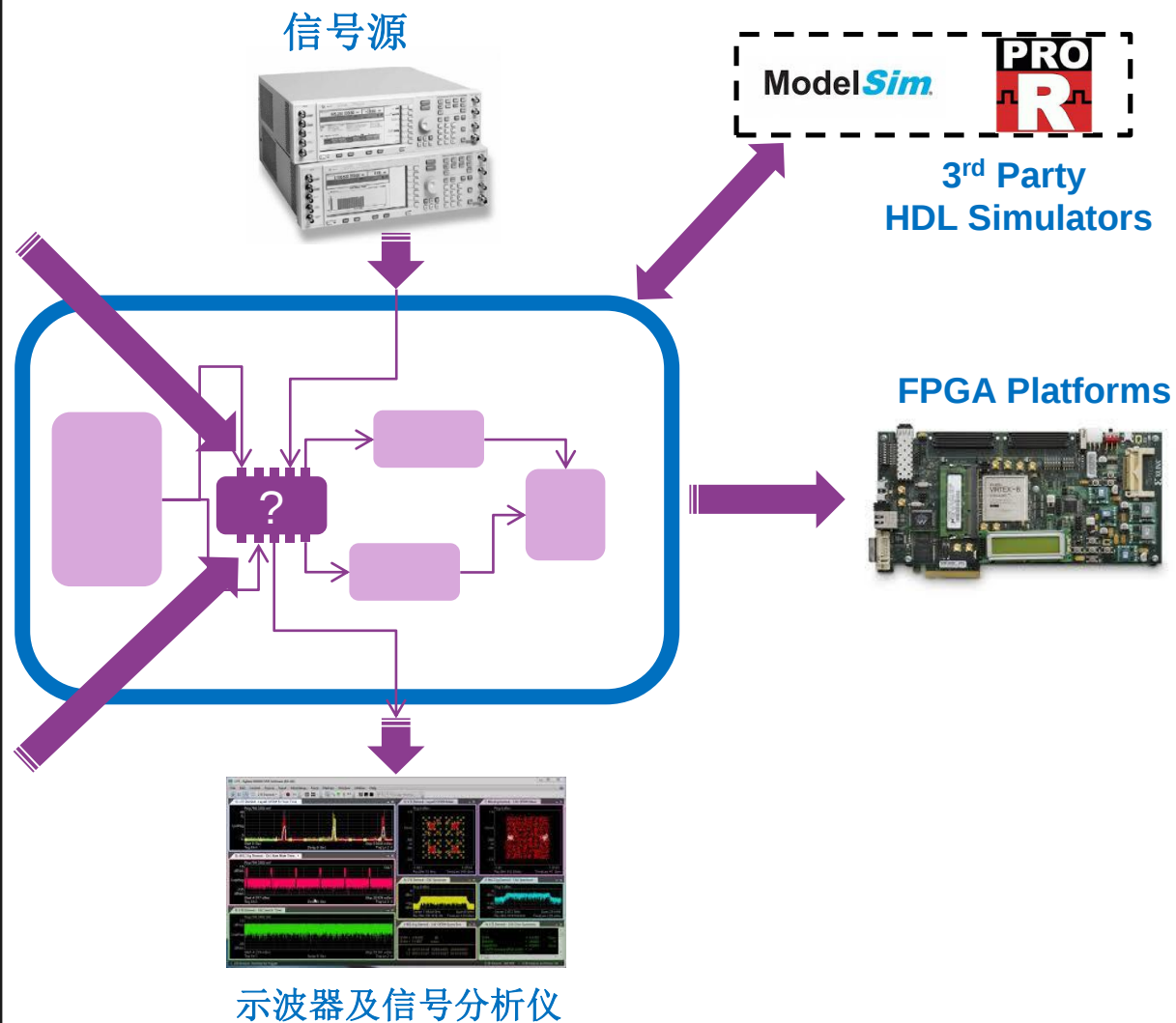
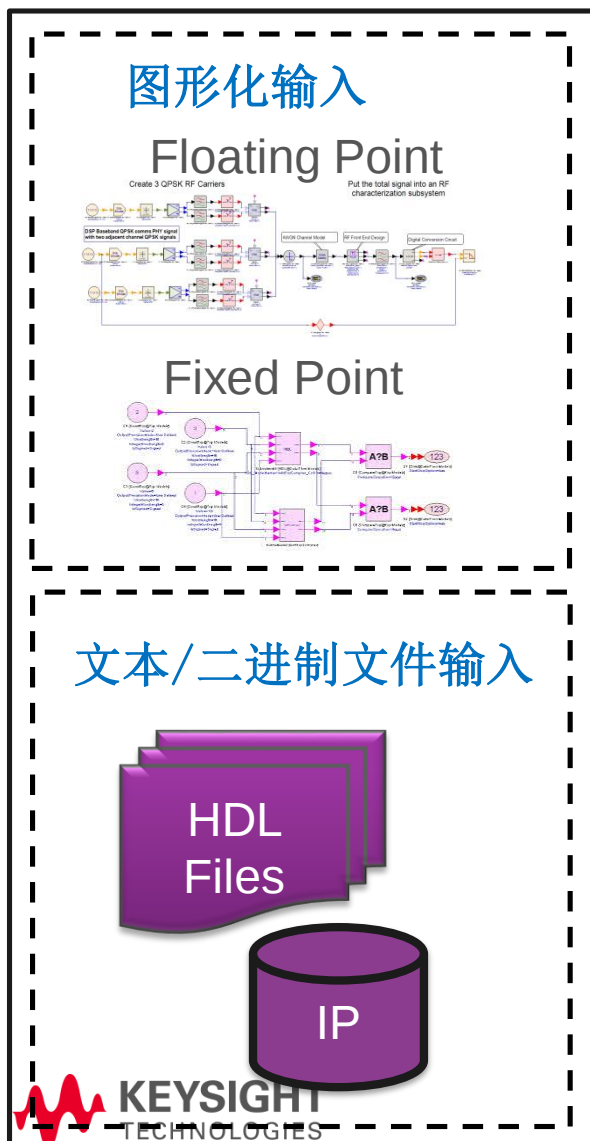


射频电路混合仿真: 1x4 Transmitter Array in ADS/Momentum

System / Circuit / EM Co-simulation and beam steering

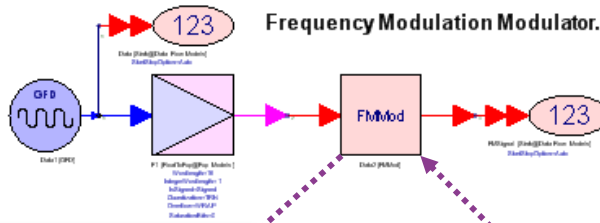


SystemVue FPGA开发流程

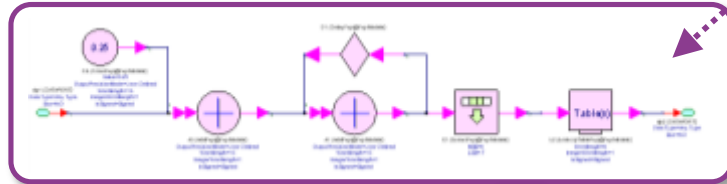


SystemVue FPGA开发流程

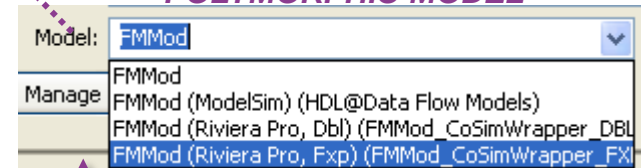
SYSTEM
LEVEL



FIXED
POINT

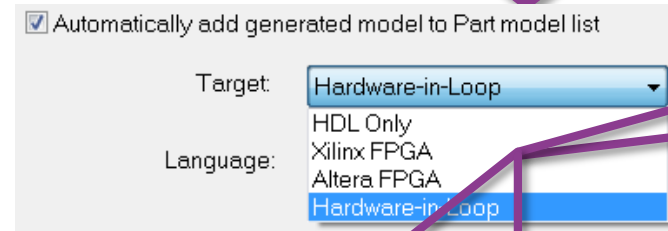


POLYMORPHIC MODEL

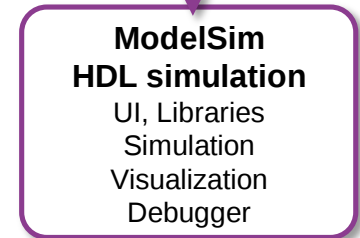
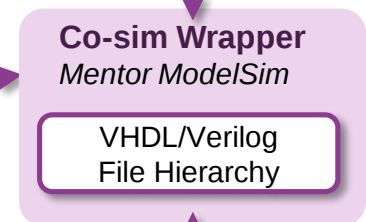
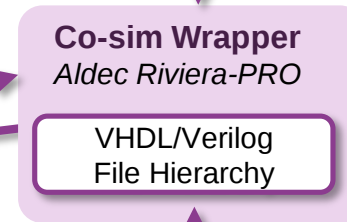
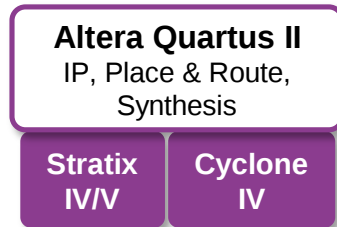


HDL Code Generator

RTL



FPGA



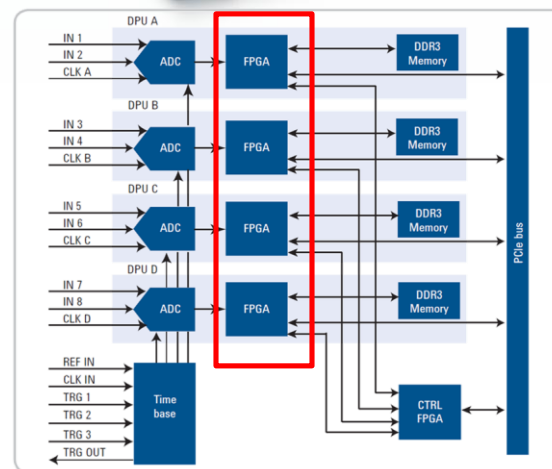
Hardware in-the-Loop (HIL)



可定制模块化测试仪表 - M9703高速数采

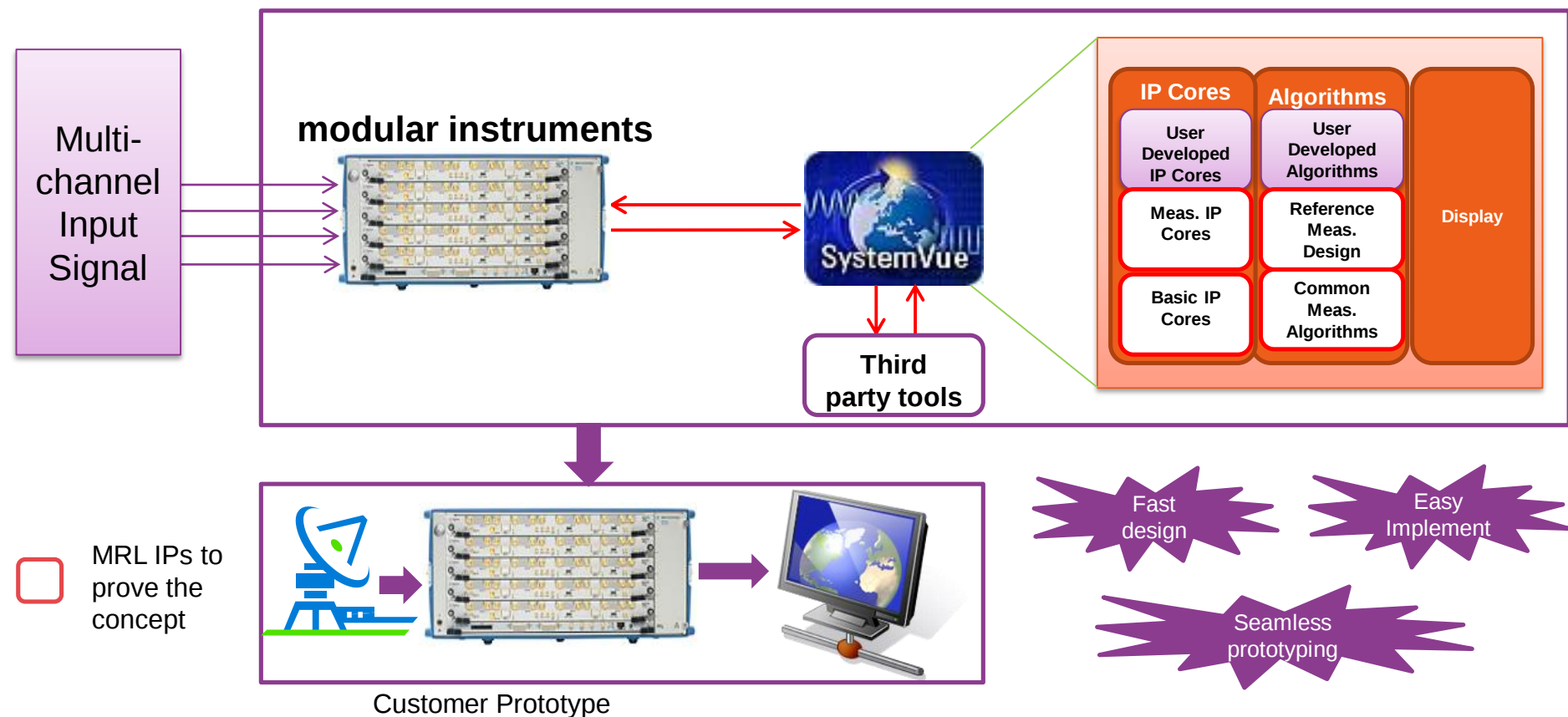
性能概况：

- 12 位比特分辨率
- 多通道相参
- 8-4 通道输入，速率高达1.6-3.2 GS/s
- 模拟带宽 DC 至 1 GHz
- 每通道存储高达 1 G 样点
- **4 片可编程 Virtex-6 FPGA**
- PCIe x4 Gen2 背板总线连接
- 支持客户定制开发 FPGA



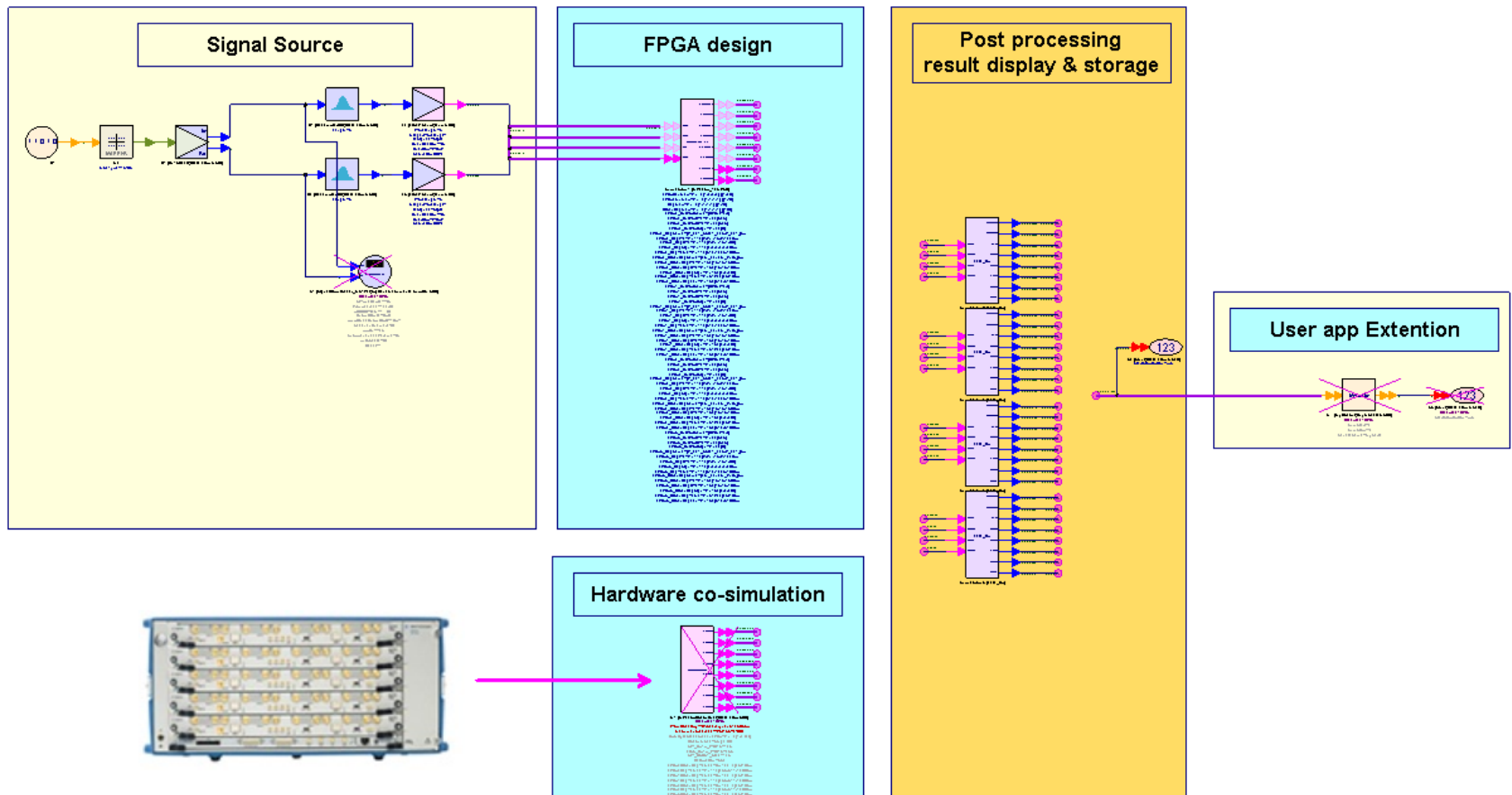
M9703A Block Diagram

使用模块化仪表+SystemVue软件进行快速原型设计



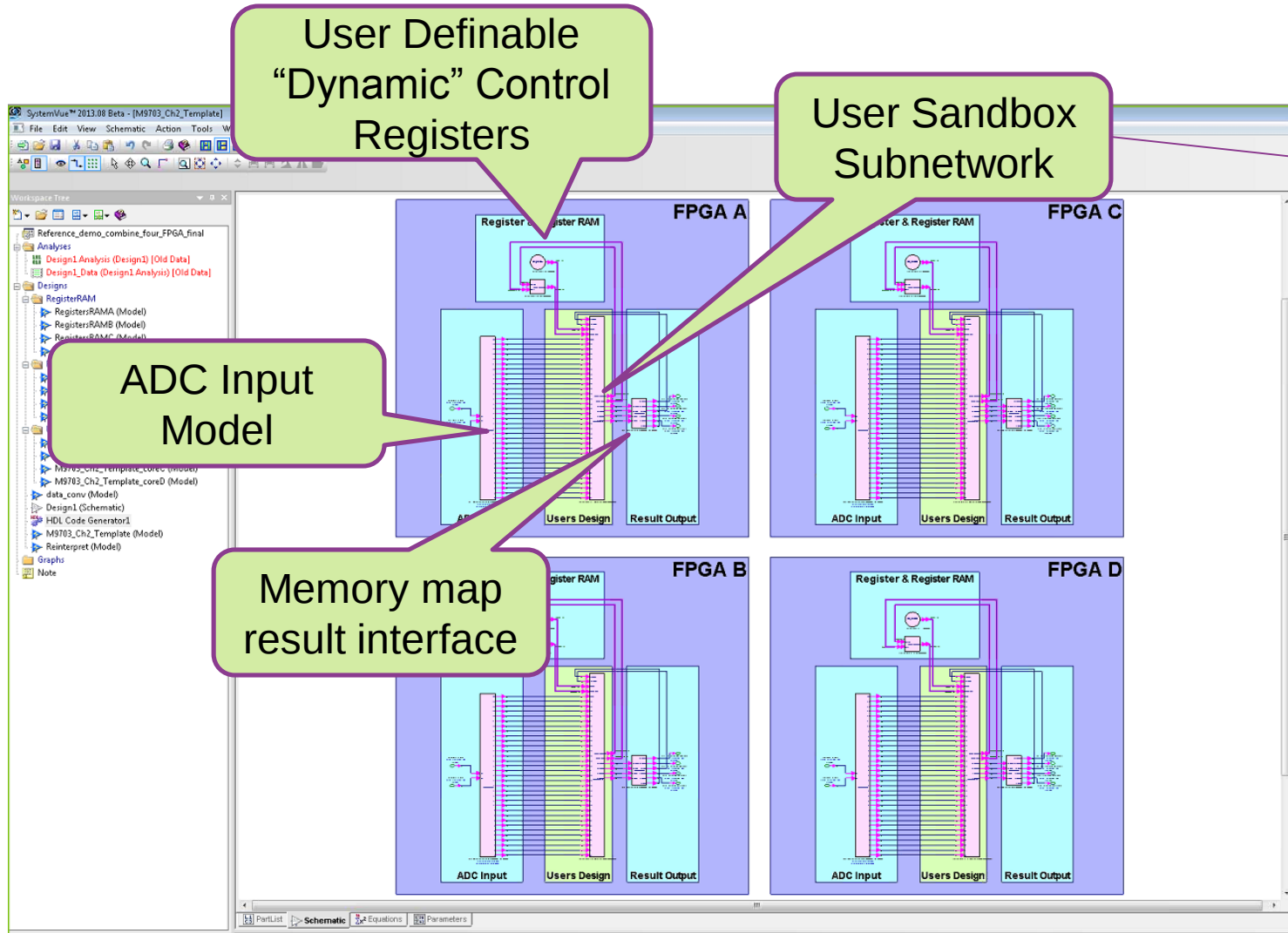
SystemVue + M9703 用户模板

Pure software simulation



Hardware co-simulation

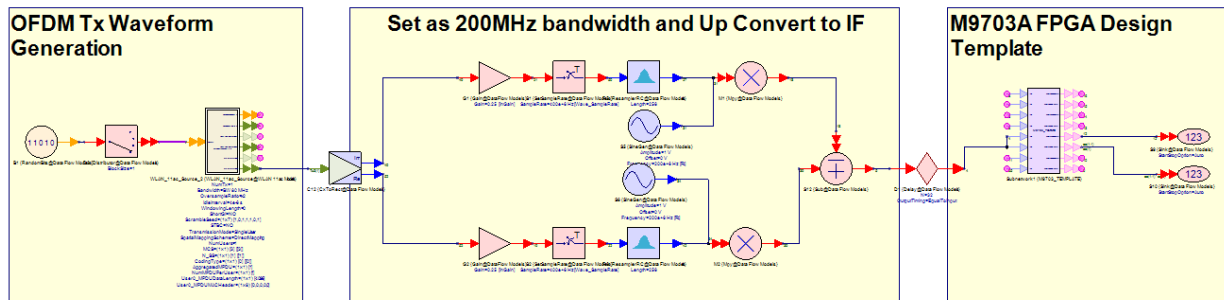
SystemVue M9703 架构



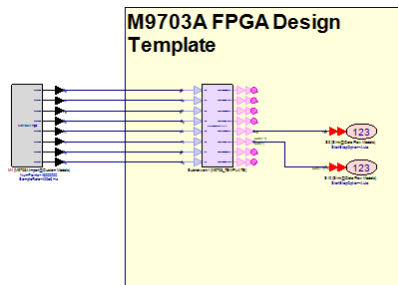
Note: Inside user sandbox, user can build a DSP algorithm using SystemVue fixed point DSP blocks, import RTL in VHDL, or even use Xilinx SystemGenerator designs. To edit the user simply pushes into this model and is given a “templated” schematic to build his algorithm.

SystemVue M9703 FPGA 开发流程

第一步： 仿真波形产生和分析



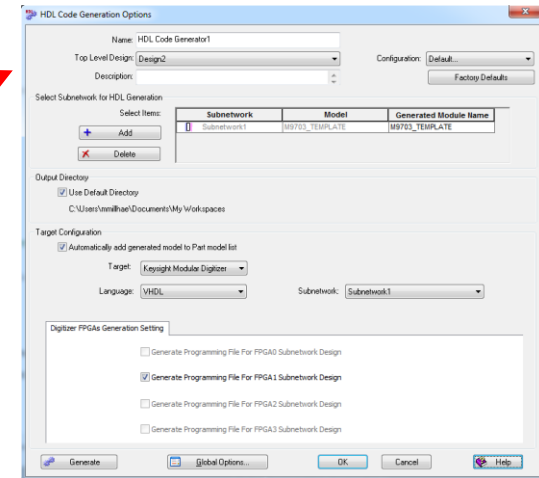
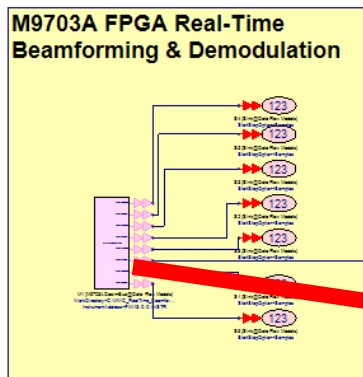
第二步：使用 M9703 进行数据捕捉，并在SystemVue中进行仿真



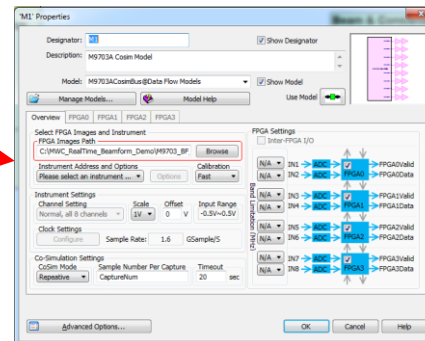
SystemVue M9703 FPGA 开发流程

第三步：生成HDL代码并综合出比特流文件

第四步：使用M9703 FPGA 硬件进行实时处理

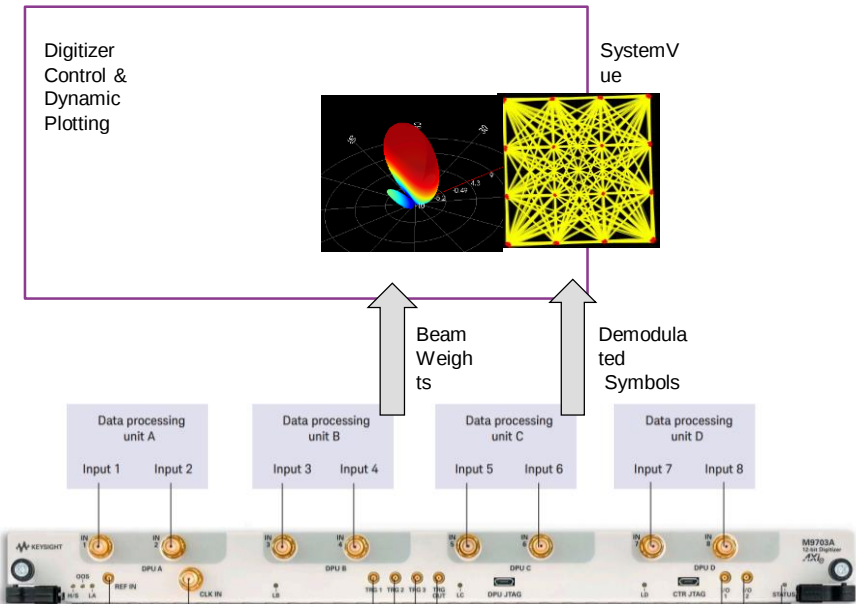
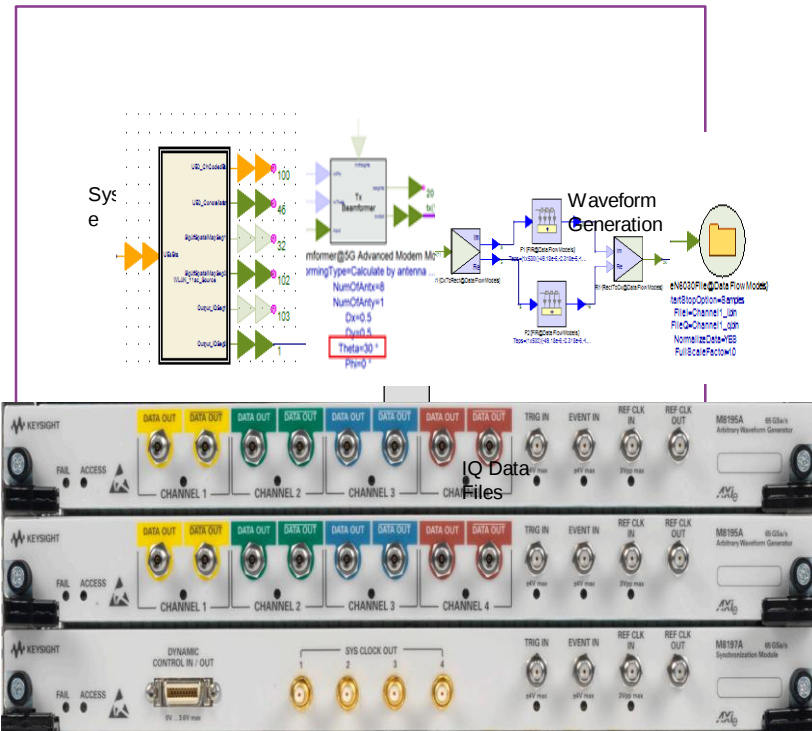


SystemVue HDL Code Generation GUI



SystemVue FPGA Configuration GUI

实时波束成形测量系统



总结

- 相控阵系统已经由传统的雷达系统走向各类通信系统中
- 相控阵系统设计是由多域的设计构成；在系统设计阶段需要将多域设计结合起来，全面分析各个单元的影响
- 是德科技EESof软件提供了基带算法、天线及射频电路及子系统的设计仿真能力，各个软件可以相互集成，协同仿真
- 层次化的设计，可以方便地将相控阵设计应用到5G/Radar/Satellite的应用场景中进行系统级分析